The Ideal Switch®

Enabling the electrification of everything
Milliwatts-to-kilowatts, DC-to-light

High-Speed Digital Products

September 2024

POWERED BY
ideal switch™

menlomicro

Company Overview

The Ideal Switch® is the most revolutionary electronics component invention since the transistor

- Company
  - Irvine, CA (HQ); Albany, NY (SUNY R&D)
  - Employees – 70+ in the US
- Capitalization
  - $228M through series C
  - Closed series C $151M Feb 2022
- Ideal Switch® in production since Q4 2020
  - 65 patent families (over 300 issued/granted)
- Innovating in critical infrastructure
  - Aerospace and Defense
  - Energy distribution
  - Telecommunications
  - Semiconductor, Capital Equipment

The Ideal Switch®

- First platform innovation in switch technology since the transistor
- Fundamental material science-based IP exclusively licensed from GE
- World's smallest, most reliable, most efficient micro-electro-mechanical switch for RF and Smart Power applications; developed over 12+ years at GE Research with another 5 years of commercialization by Menlo Micro

Our investors

standard investments, PALADIN, FUTURESHAPE, VERTICAL VENTURE PARTNERS, PIVA, DBL PARTNERS DOUBLE BOTTOM LINE VENTURE CAPITAL, Fidelity, Adage

The Ideal Switch® Story

The Ideal Switch® is the most revolutionary electronics component invention since the transistor

1879

Edison patents the circuit breaker

1892

General Electric formed, combining Edison's various companies

Over 100 years of experience in high voltage, high reliability industrial controls

2004

GE starts effort to reinvent the circuit breaker with a MEMS switch

GE develops core IP, including high temperature, high reliability metal alloy science

2016

Menlo Microsystems is formed

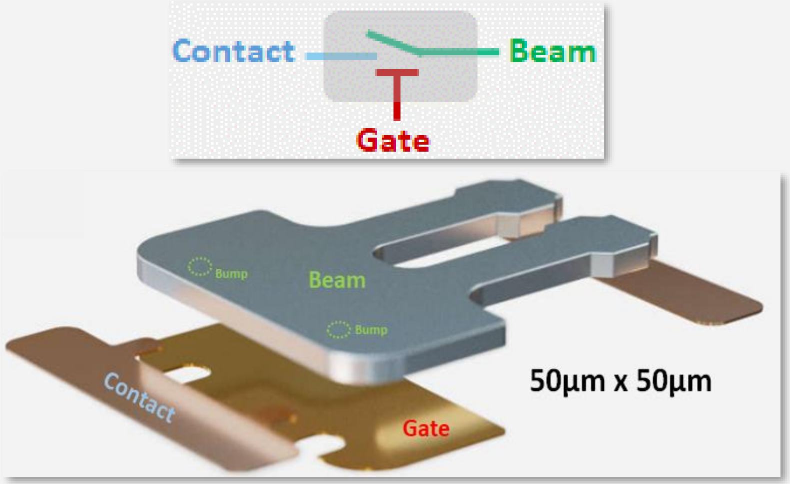
Menlo Microsystem's Ideal Fab™ Long-Term Fabrication Strategy Addresses Capacity, Efficiency, and Supply Chain Consolidation

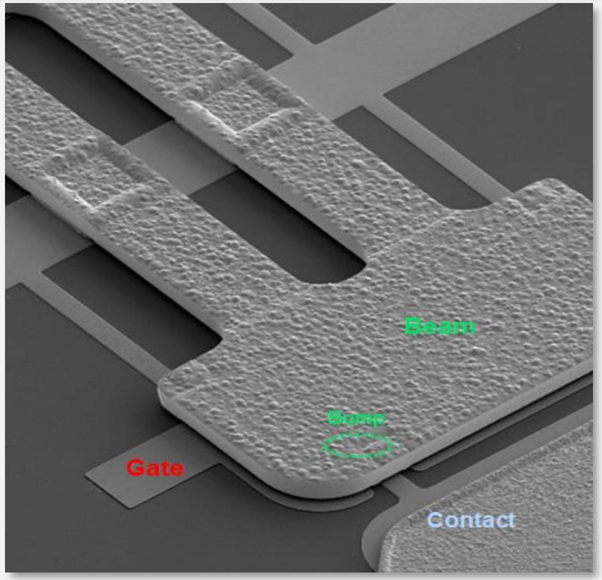
- ***Announced on 11th July 2024***
- ***Up to 2k wafer per month capacity***
- ***Highlights of new Ideal Fab***
  - *Onshore the Ideal Switch technology*
  - *Manage and control Menlo Microsystems supply chain*
  - *Planning a Glass Center of Excellence*

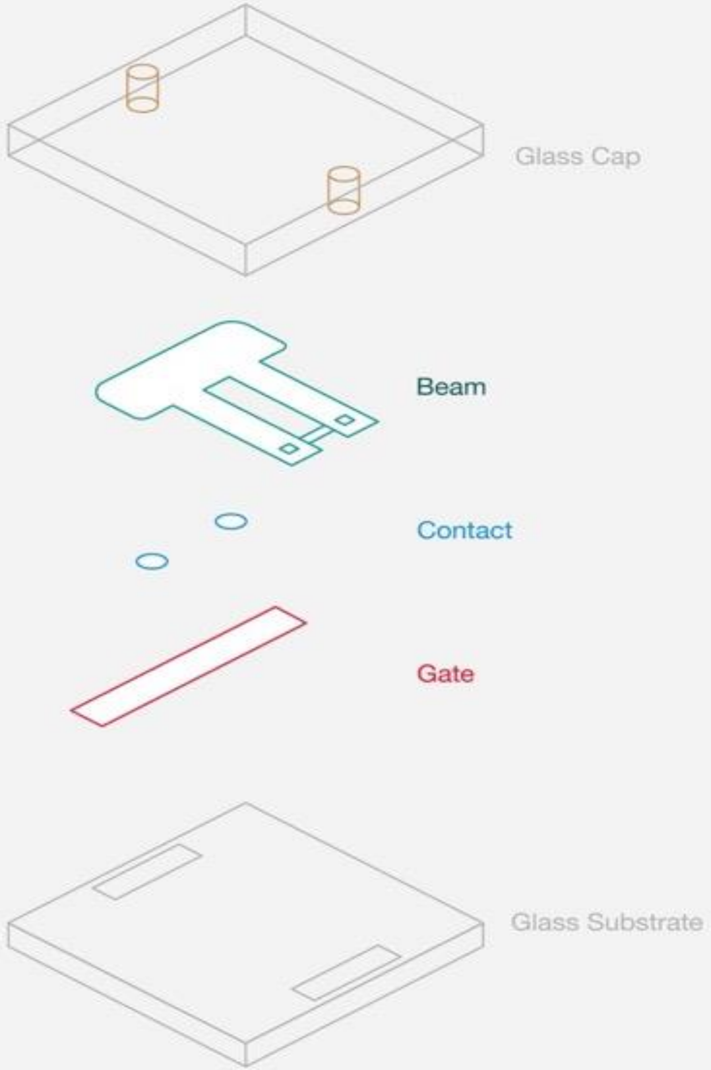
Menlo Microsystems Announces Deal to Manufacture the Ideal Switch® in Upstate New York, Commits to Multi-Year Investment of $150 Million to Fully Onshore Production

How Ideal Switch® Works – The Unit Cell

Technology platform with breakthrough innovations in materials and processing







Ideal Switch Technology - How It Works | Menlo Micro

Unique Beam & Contact Glass Substrate

- High RF power
- Low insertion loss
- High linearity
- Long life

System-In-Glass (SiG)

- Through-glass-vias
- High frequency
- Low parasitics
- Hermetically sealed

Scalability

- 50 µm x 50 µm unit-cell
- Scalable 2D switch array (voltage, current, power, frequency)

Configurability

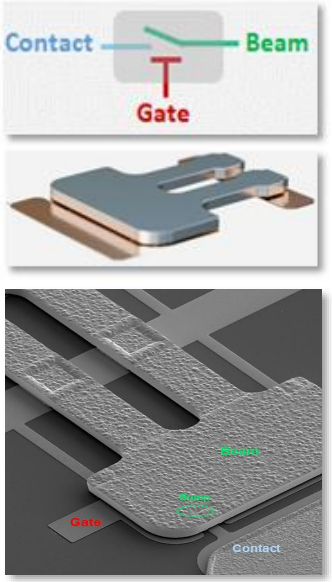
- 2D switch array
- Configurable for M-poles, N-throws

System-In-Package (SiP)

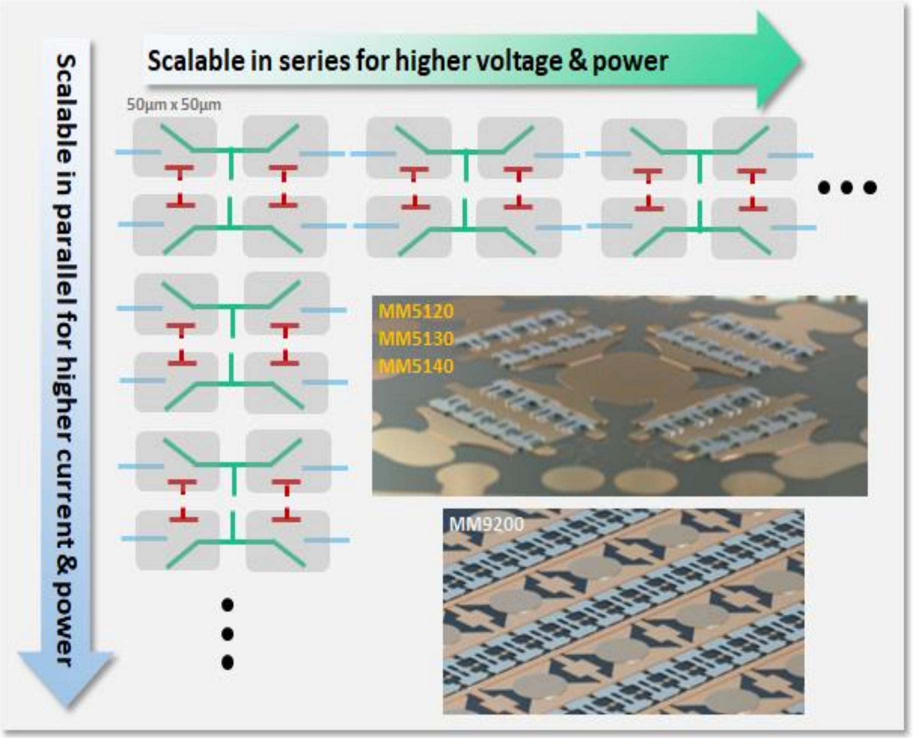
- 2D array integrated with CMOS driver and passives

Scalable Switch Arrays With Ideal Switch®

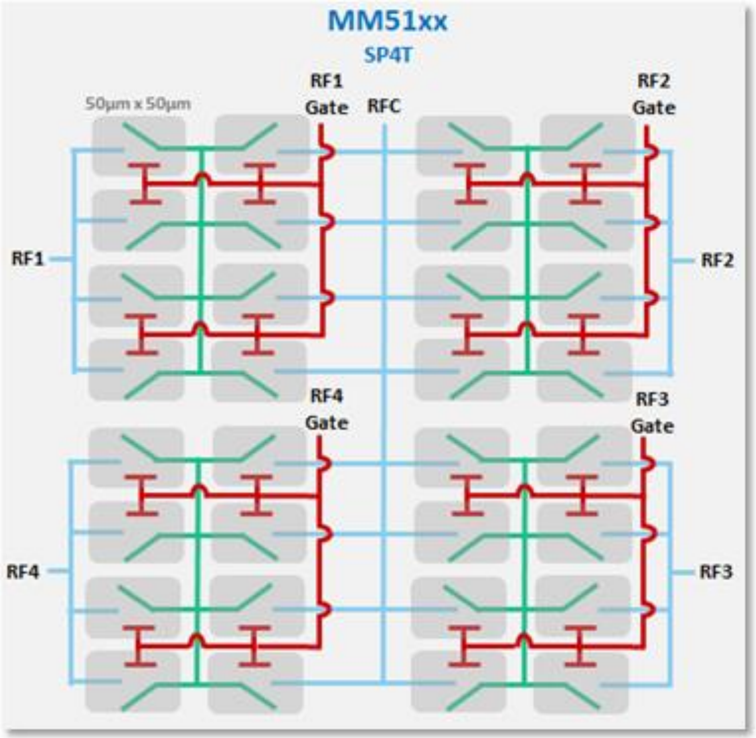
Unit Cell
50µm x 50µm

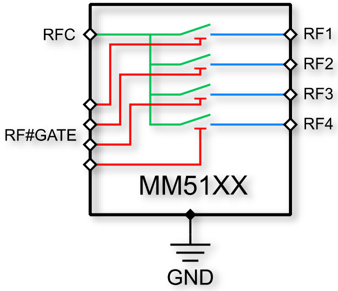


2D
Scalability

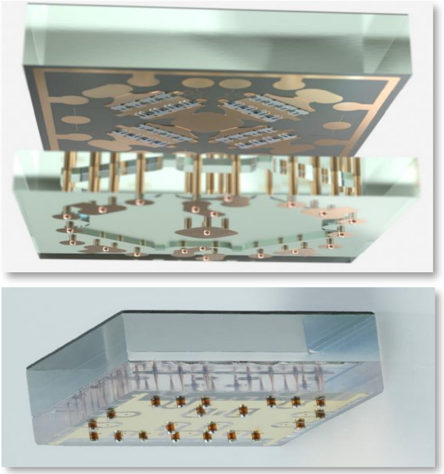


Switch
Portfolio





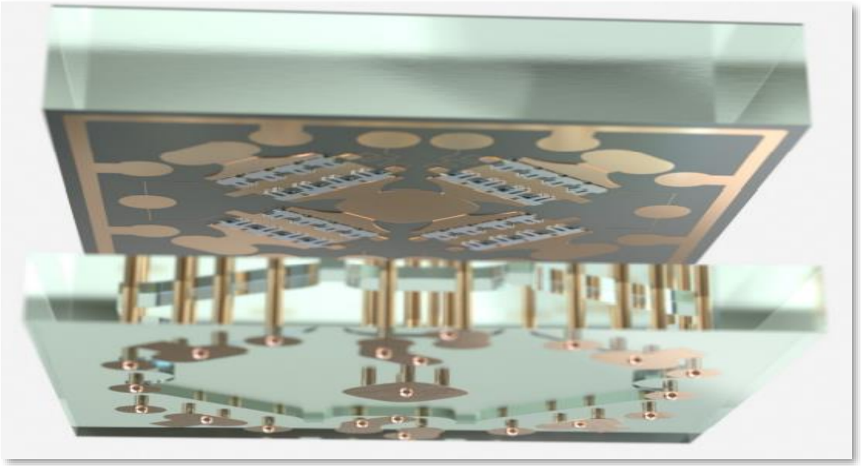
System In Glass
SiG

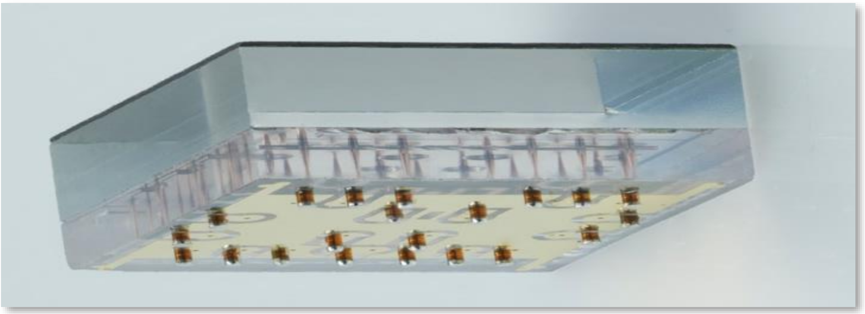


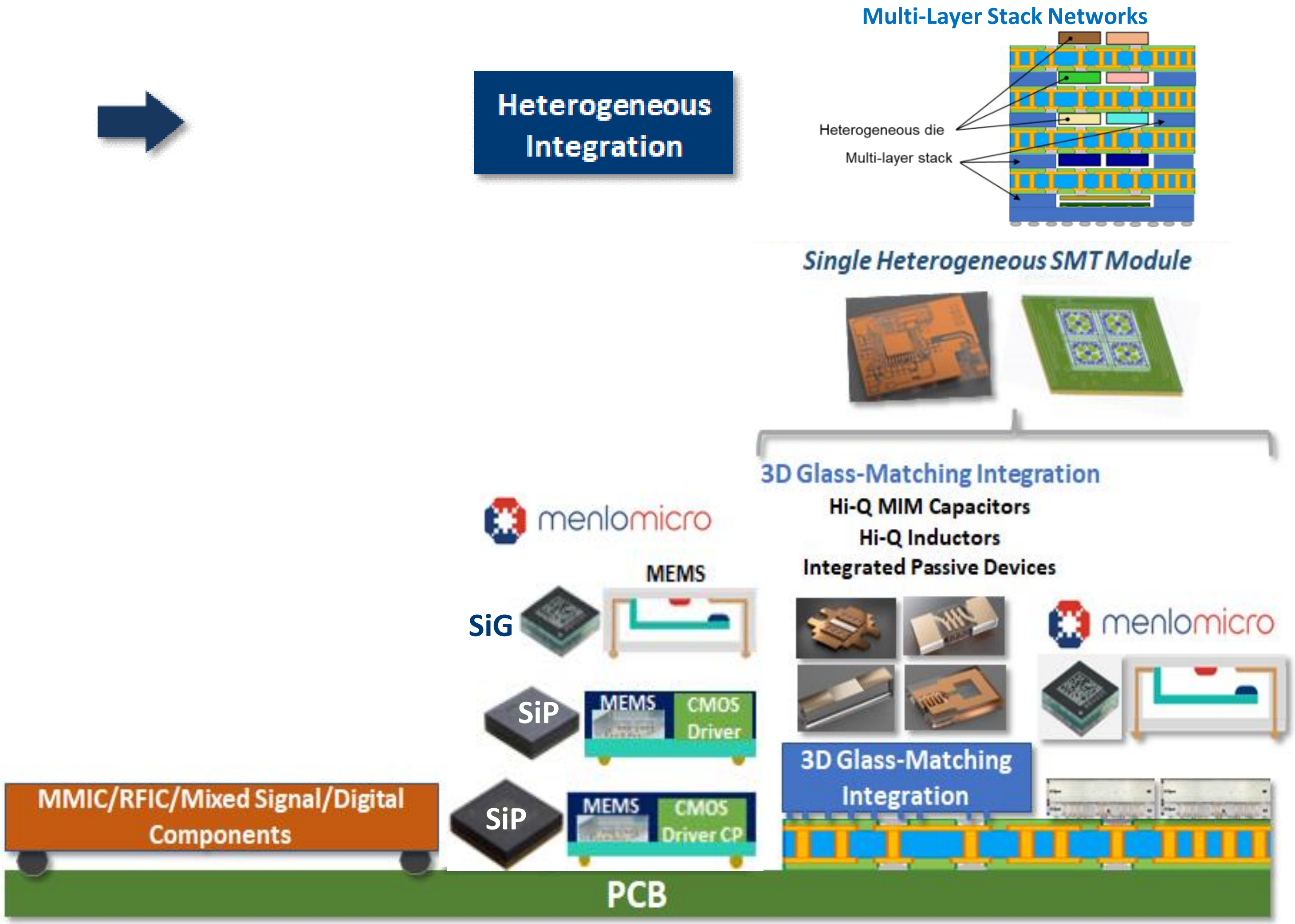
Heterogeneous Integration With System-In-Glass

System-In-Glass
SiG

Heterogeneous Integration







SiG = System-In-Glass
SiP = System-In-Package

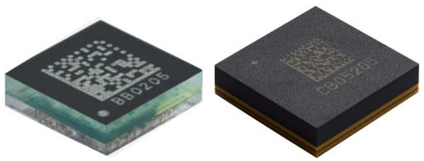
[RF Switch Matrix | RF Subsystems from Menlo Micro](#)

Advantages of Ideal Switch® - Seven Pillars of Advantages

*The Ideal Switch® inherits the best of both worlds with **Seven Pillars of Advantages** when compared with popular RF switch technologies across leading suppliers*

- ***High RF power handling*** – up to 25 W/150 W (CW/pulsed)
  vs solid-state
- ***Low insertion loss*** – less than 1 dB
  vs solid-state
- ***High linearity*** – unmatched >90 dBm IP3
  vs solid-state and electromechanical
- ***Fast Switching*** – less than 20 µs
  vs electromechanical
- ***Long life*** – minimum 3 billion switch cycles
  vs electromechanical
- ***Low DC power*** – from 0.1 mW to less than 10 mW
  vs electromechanical and solid-state
- ***Small size*** – from 6 mm^2 to 22 mm^2 footprint
  vs electromechanical

POWERED BY ideal switch™



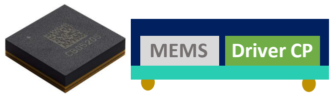
Low Cost of Ownership

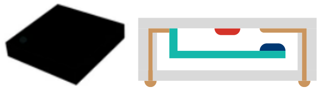
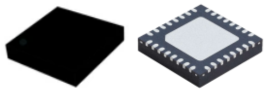
Product Portfolio – High Frequency

	RF & Microwave			High-Speed Digital	
Model	**MM5130**	**MM5120**	**MM5140**	**MM5600**	**MM5620/MM5622**
Markets	Telecommunication, Wireless Aerospace & Defense, Test & Measurements			Semiconductor Test & Measurement, Automated Test Equipment, Aerospace & Defense Equipment	
Applications	Tunable & Programmable Filters, High-Power Low-Loss RF Switch Matrices, Programmable RF Steering Components, Switchable & Tunable RF Components			High-Speed Digital SoC Testing & Signal Routing Optical-Electrical Module & Switch Matrix Testing	
Specifications					
Switch Type	SP4T			DPDT	2x DP3T
Frequency Range	DC – 26 GHz	DC – 18 GHz	DC – 8 GHz	40 Gbps	64 Gbps
RF Power	25 W (CW), 150 W (pulsed)			---	
Insertion Loss	0.4 dB @ 6 GHz	0.4 dB @ 6 GHz	0.3 dB @ 3 GHz	1.3 dB @ 10 GHz	1.5 dB/1.1dB @ 16 GHz
Linearity (IP3)	>90 dBm			---	
Control	Direct	SPI/GPIO	SPI/GPIO	SPI*	SPI/GPIO
DC Supply	89 V (gate)	3.3 V (control), 5 V ($V_{booster}$)		5 V (control), 89 V (gate)	3.3 V (control), 5 V ($V_{booster}$)
Lifetime	>3B cycles			> 3B cycles	
Package	2.5 mm x 2.5 mm WLCSP	5.2 mm x 4.2 mm LGA		8 mm x 8 mm LGA	8.2 mm x 8.2 mm LGA
Availability	In production			In production	

*SPI control signals: data, clock, latch, blank

Product Portfolio – Power Management



	Signal Relay	Smart Power & Management	
Model	**MM1205**	**MM9200**	**MM101**
Markets	Test & Measurement, Wireless Charging, Scientific & Medical, Telecommunication	Industrial Automation, Sustainable Buildings Transport Electrification, Infrastructure Modernization	
Applications	High-Density Switch Matrices, Automated Test & Measurement, Mechanical & Photo Relay Replacement	LV Industrial Controls Solid-State & Electromechanical Relay Replacements	
Specifications			
Switch Type	6x SPST	SPST	8-channel high voltage booster & control
DC Current	1 A per channel, 2 A per device	10 A (AC or DC), 10 mΩ	
DC Carry/Standoff Voltage	38 V or 30 V*/100 V	300 V (AC or DC)	---
Frequency Range	DC – 3 GHz	---	---
Control	SPI/GPIO	Direct	SPI/GPIO
DC Supply	3.3 V (control) 5 V ($V_{booster}$)	90 V (gate)	3.3 V (control) 5 V ($V_{booster}$)
Lifetime	>3B cycles	1B cycles	---
Package	8 mm x 8 mm LGA	5 mm x 5 mm WLCSP 6 mm x 6.5 mm QFN	5 mm x 5 mm QFN 1.6 mm x 2.4 mm WLCSP
Availability	**In production**	**Samples: Available** **Production: Q1 2025**	**In production**

*38V (using external 100V driver), 30V (using integrated driver)

Product Roadmap

Driving and accelerating product roadmap from customers applications

	Current Product Portfolio	Future Product Roadmap
RF & MICROWAVE SWITCHES	**MM5130** DC-26GHz 25W, SP4T **MM5120** DC-18GHz SP4T w/CP **MM3105** DC-3GHz 6xSPST w/CP **MM5140** DC-8GHz SP4T w/CP **MM3100** DC-3GHz 6xSPST **MM5810** RF Limiter SPST	**MM5800** 70GHz SP2T • Higher frequency • Lower return loss, higher isolation • Higher cycling lifetime at 85C°
HIGH-SPEED DIGITAL SWITCHES	**MM5600** 40Gbps DPDT **MM5620** 64Gbps Dual DPDT w/CP	**MM56xx** 128Gbps • Higher data rate (beyond PCIe 6…) • Smaller form factor, higher density • Custom/multichip switch configurations
POWER MANAGEMENT SWITCHES	**MM101** 8CH Driver Charge Pump **MM1200** 1A,13V_{CV} 6xSPST **MM9200** 300V/10A SPST **MM1205** 1A, 40V_{CV} 6xSPST w/CP	**MM92xx** Monitor Protect Control • Higher carry voltage & current • Lower R_{ON} • Lower leakage current • Integrated power solution

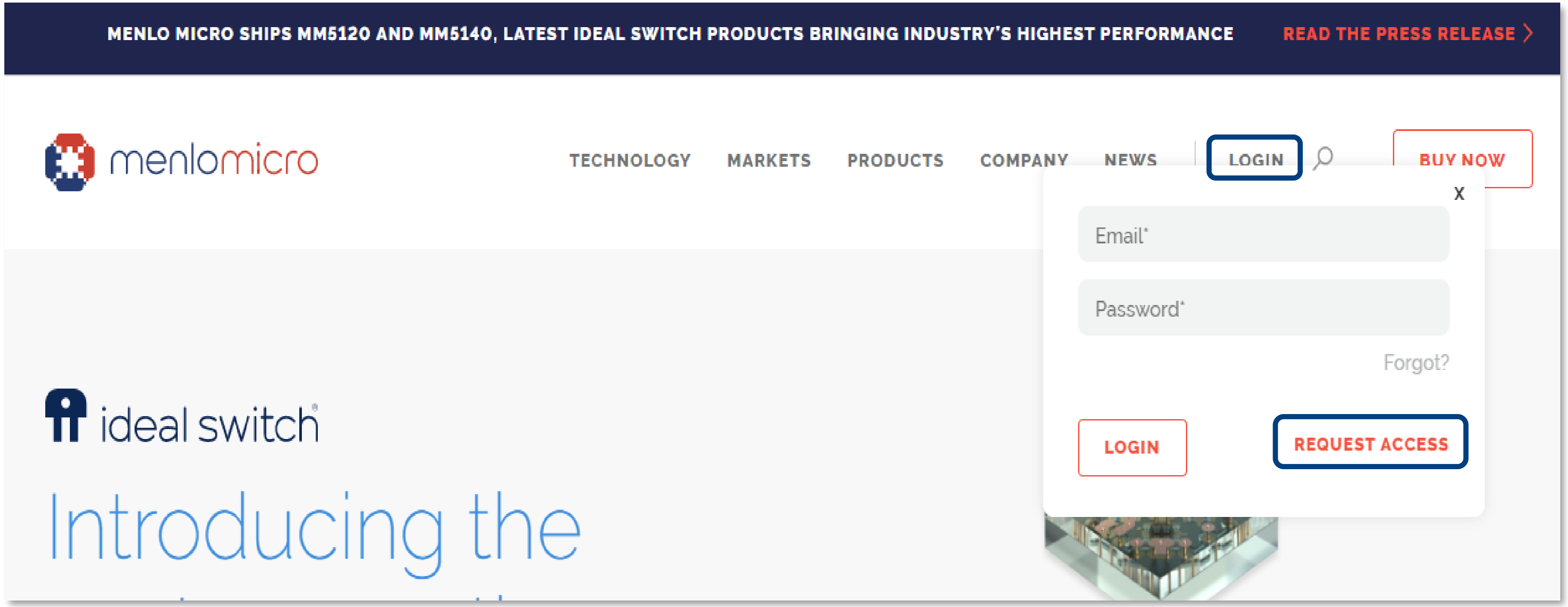
RF & MICROWAVE REFERENCE DESIGN	**MM4xxx** DC-18GHz Switch Matrix Systems
	MM61xx DC-18GHz, TDU Phase Shifters
		Heterogeneous Integration
		Time Delay Unit Wideband, Low Loss, High Linearity
		• Ideal switch® as core elements for
		  • System-in-package (SiP) heterogeneous integration with RF/digital/mixed signal ICs
		  • 3D glass matching integration with passive devices
		  • Switch module integration
		  • Time delay unit integration

Website Resources

Additional product support and documentation on website

- **Users can sign up by clicking on “Login” and then “Request Access”**
- **Access is typically granted within 24hrs**

http://www.menlomicro.com

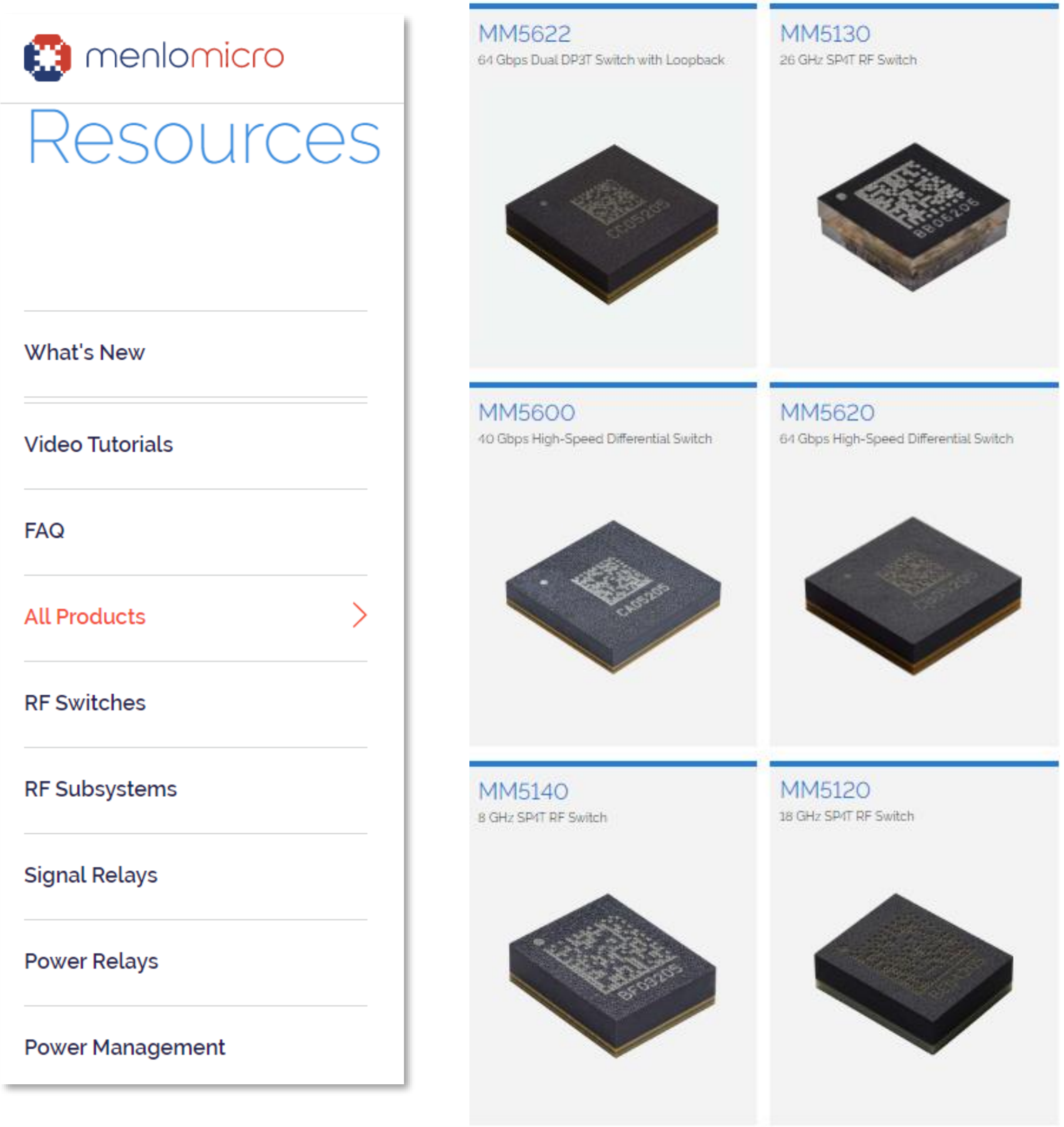


Website Resources

Once logged in you will find:

Design and Product Collateral Resources

- Product Briefs
- Application Notes
- Qualification Reports
- S-Parameters
- Transmission Line Models
- CAD Drawings
- Assembly Instructions
- RoHS/REACH Certificates
- Eval Board GUI
- Eval Board Instructions
- Video Tutorials
- FAQs
- Product Images



The Ideal Switch®

MM5620/MM5622 – 64 Gbps High-Speed Differential Switch

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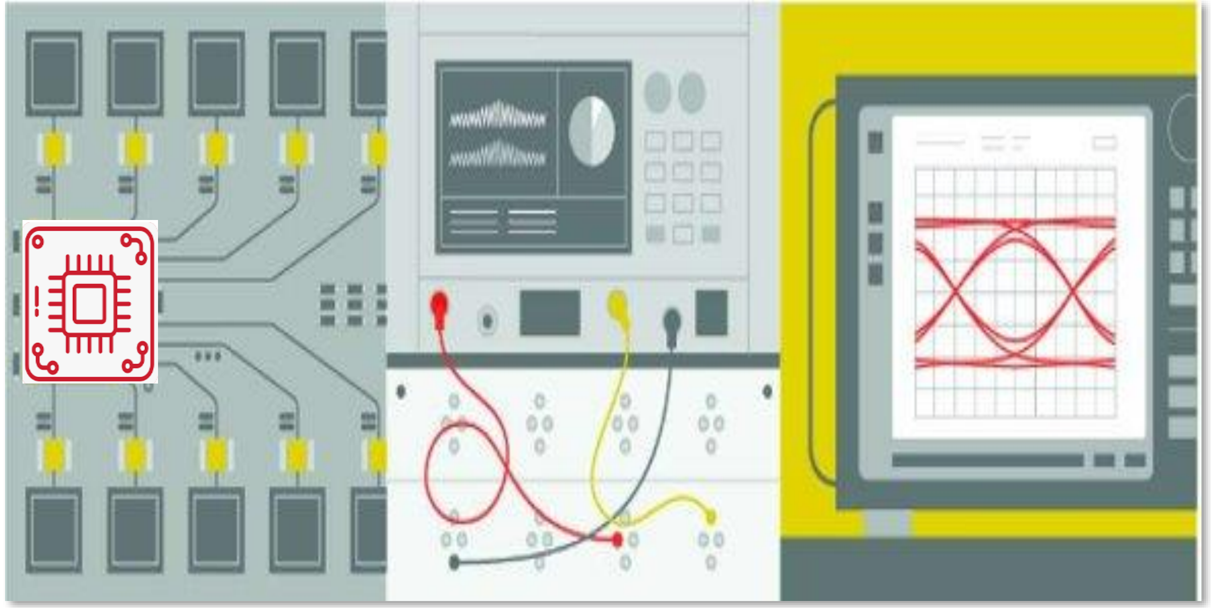
MM5620/MM5622 – Target Markets & Applications

Target Markets

- Automated Test Equipment
- Measurement Equipment
- Semiconductor Final Package Testing
- Compliance and Loopback Testing
- Aerospace & Defense Equipment



Target Applications

- High-Speed Digital SoC Testing

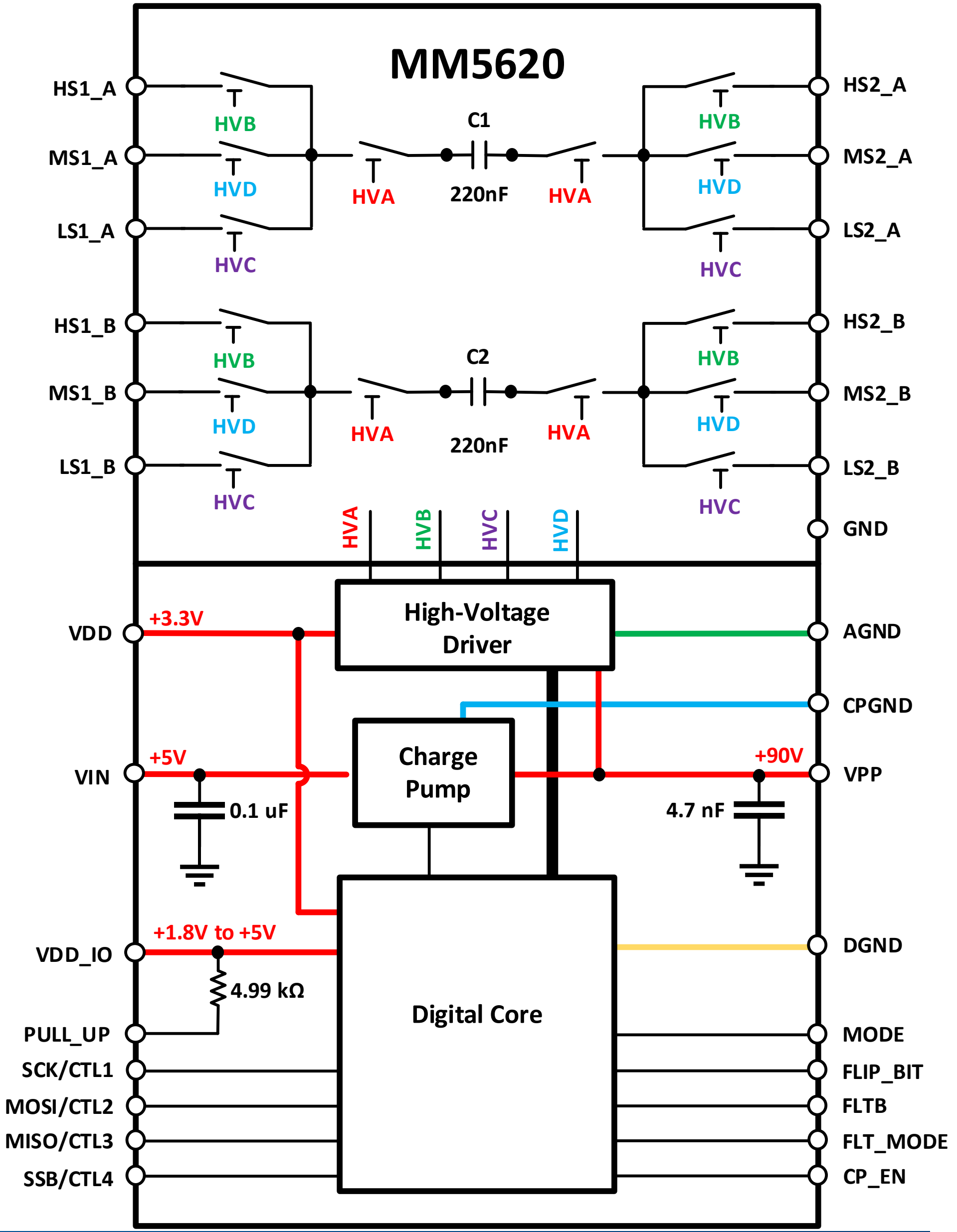
  PCIe Gen 5 & 6, SerDes, USBx.x, InfiniBand, HDMI…
- Optical-Electrical Module Testing
- High Speed Signal Routing
- Differential Switch Matrices

MM5620 – Product Highlights

- Dual 2 Form C DP3T Differential Loopback Mode
- DC to 20 GHz range
- DP3T (differential mode) with Loopback Mode
- Integrated charge pump & high-voltage driver
- Power supply 5 V (voltage booster) 3.3 V (analog)
- SPI and GPIO interface
- Built-in passive components
  - DC blocking capacitors
  - Internal VPP capacitor
  - Internal 4.99k pullup resistor
  - Internal 0.1uF/10V VIN to CPGND bypass capacitor
- High reliability >3B switching cycles
- 8.2 mm x 8.2 mm LGA

[Menlo MM5620 Datasheet (menlomicro.com)]

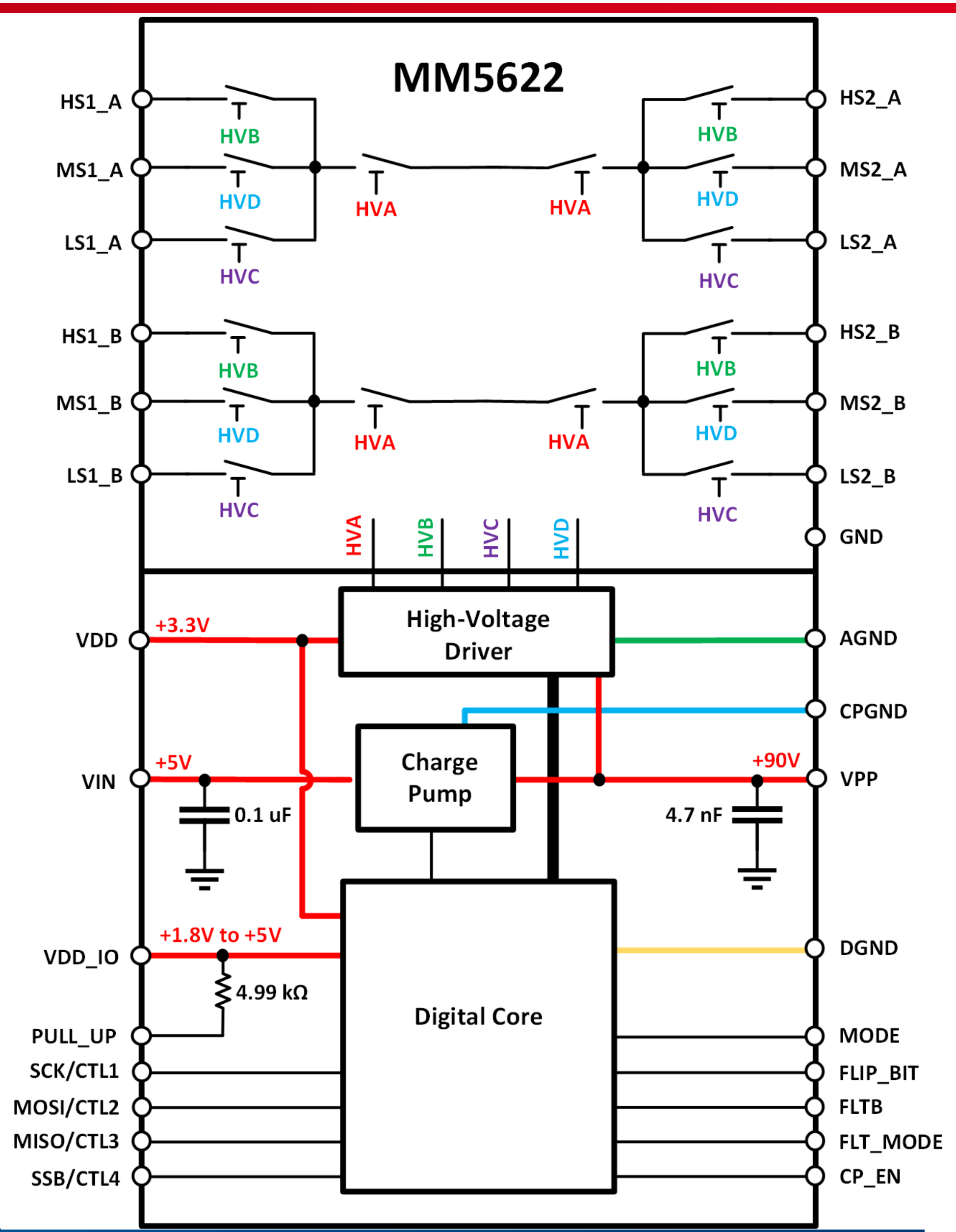
[MM5620-01NDB_Qual_and_Characterization_Report_Rev-1.pdf (menlomicro.com)]



MM5622 – Product Highlights

- MM5622 supports DC-coupled signal paths only
- Dual 2 Form C DP3T Differential Loopback Mode
- DC to 20 GHz range
- DP3T (differential mode) with Loopback Mode
- Integrated charge pump & high-voltage driver
- Power supply 5 V (voltage booster) 3.3 V (analog)
- SPI and GPIO interface
- Built-in passive components
  - Internal VPP capacitor
  - Internal 4.99k pullup resistor
  - Internal 0.1uF/10V VIN to CPGND bypass capacitor
- High reliability >3B switching cycles
- 8.2 mm x 8.2 mm LGA

https://menlomicro.com/images/general/MM5622_Datasheet.pdf



MM5620/MM5622 - Functional Block Diagram

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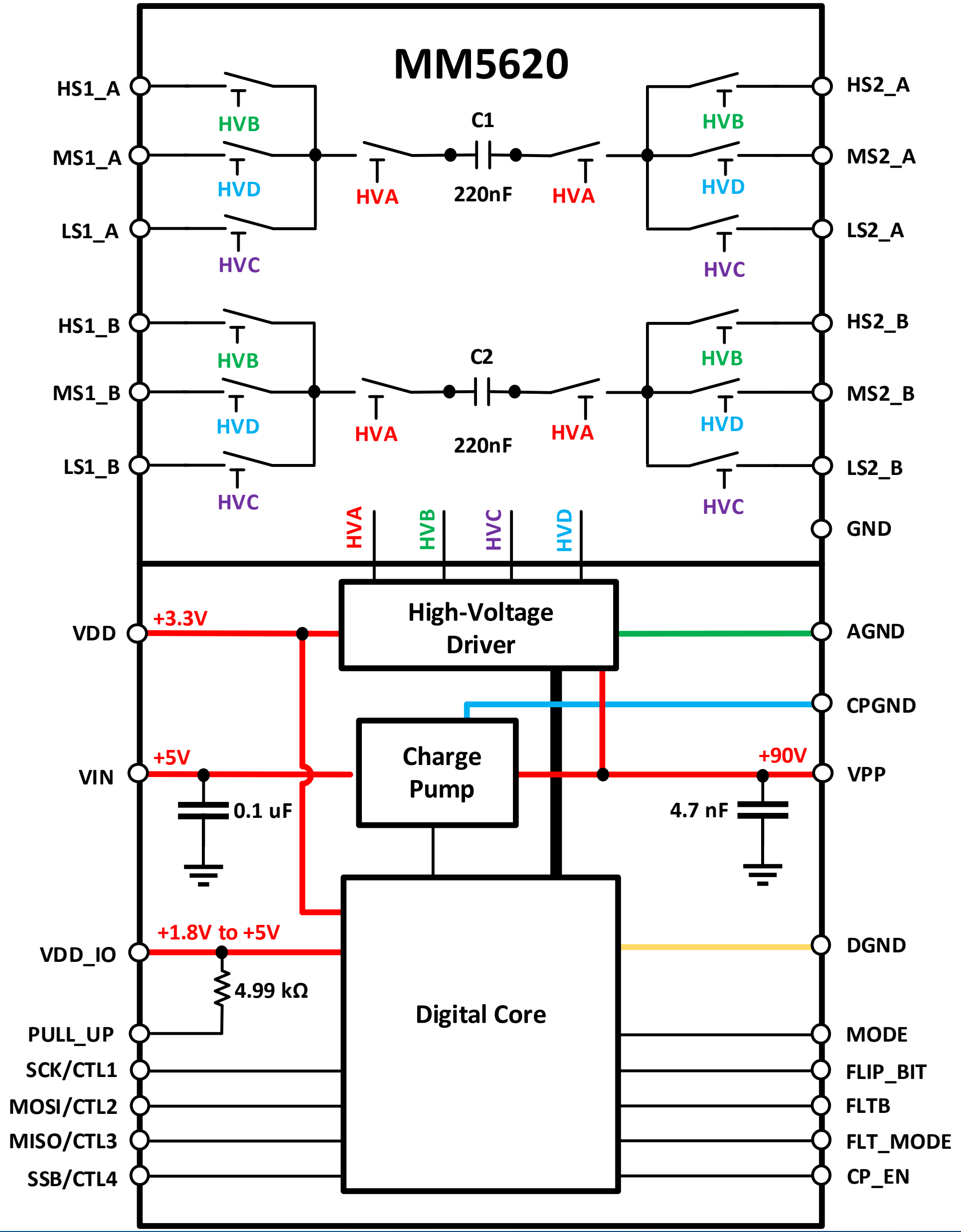
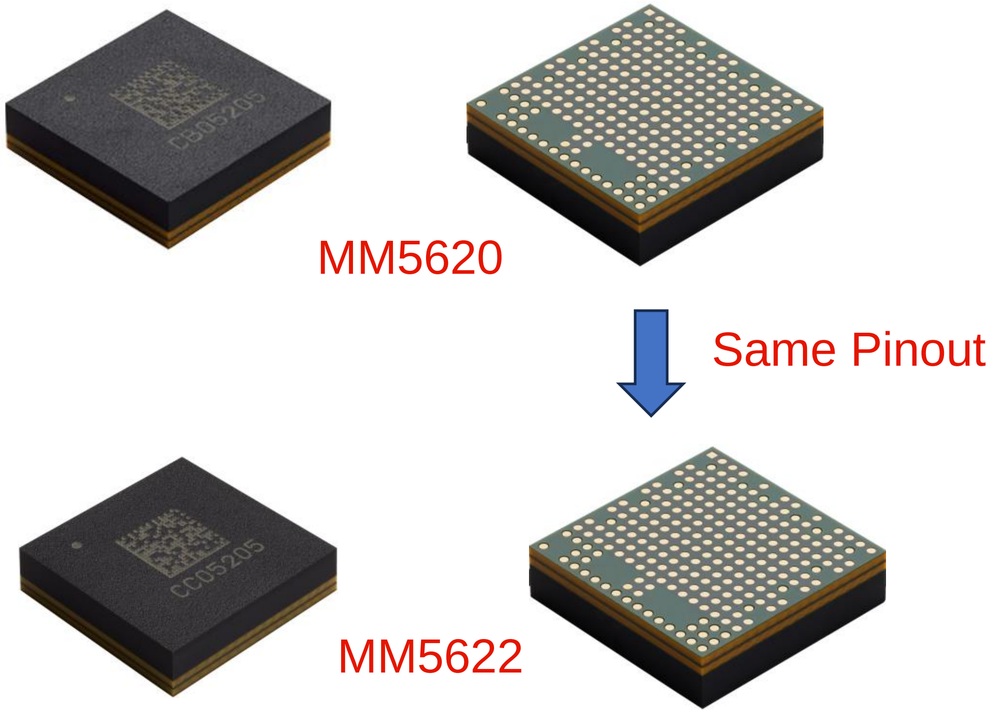
- Differential, Dual DP3T
- High-speed (HS) loopback path supports 64 Gbps
- Flexible functionality
  - HS1 → HS2 (loopback)
  - MS1 → MS2 (loopback)
  - HS1 → MS1 (ATE)
  - HS2 → MS2 (ATE)
  - HS → LS (ATE)
  - MS → LS (ATE)
  - LS → LS (LS loopback)

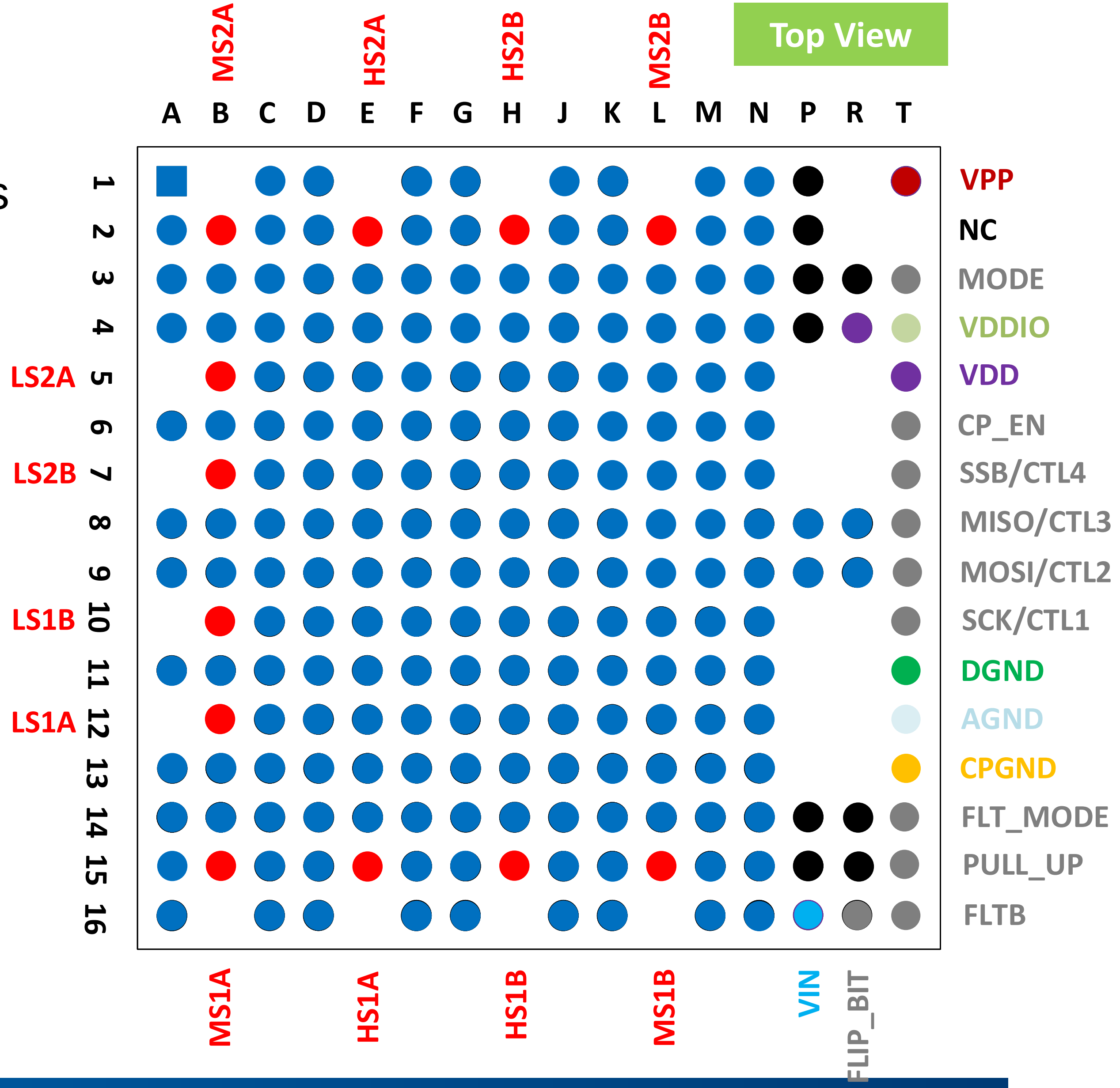
HS = high-speed path
MS = medium-speed path
LS = low-speed path



MM5620/MM5622 - LGA 16x16 Footprint Diagram

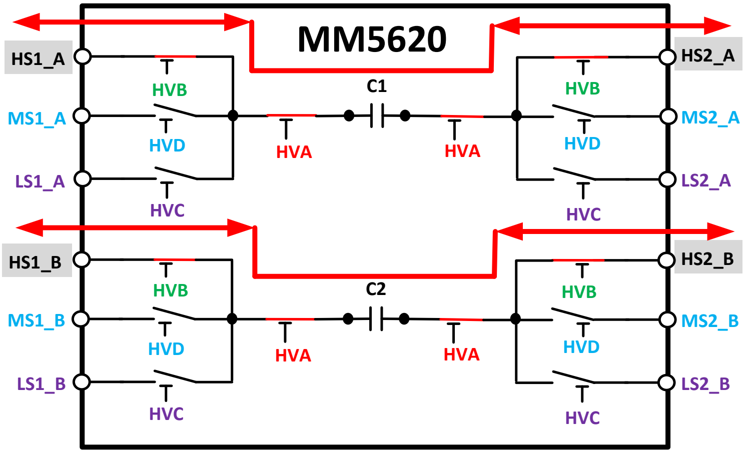
- Size: 8.2 x 8.2 mm^2
- 0.5 mm pitch / 0.3 mm pad diameter
- 16x16 LGA array – with removed pads as needed





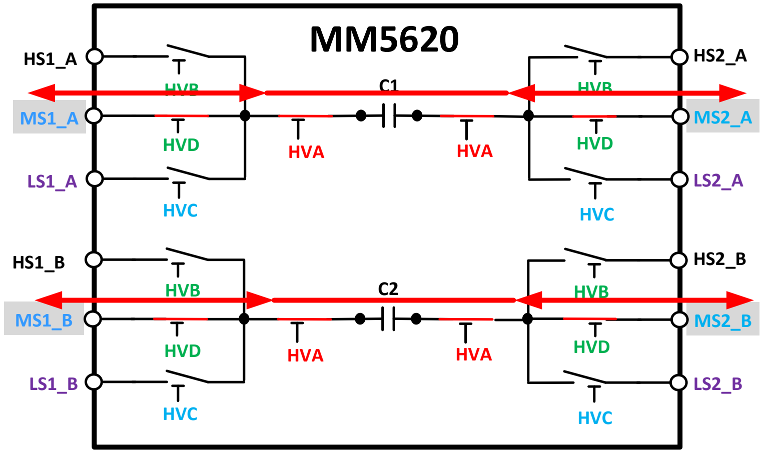
MM5620/MM5622 – Six Signal Paths

- Three signal paths going through the AC- coupling capacitors for the MM5620 device
- The same DC-coupled signal paths supported for the MM5622 device
  - Case 1: High Speed 1 to High Speed 2
  - Case 2: Medium Speed 1 to Medium Speed 2
  - Case 3: Low Speed 1 to Low Speed 2



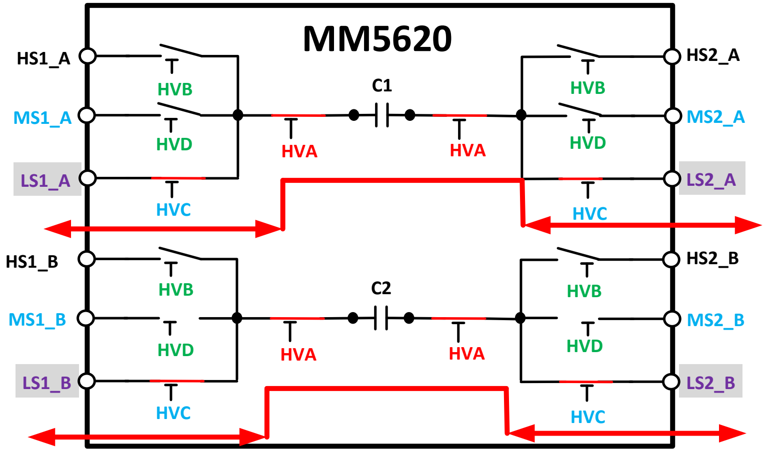
HS1 ↔ HS2

Case 1



MS1 ↔ MS2

Case 2

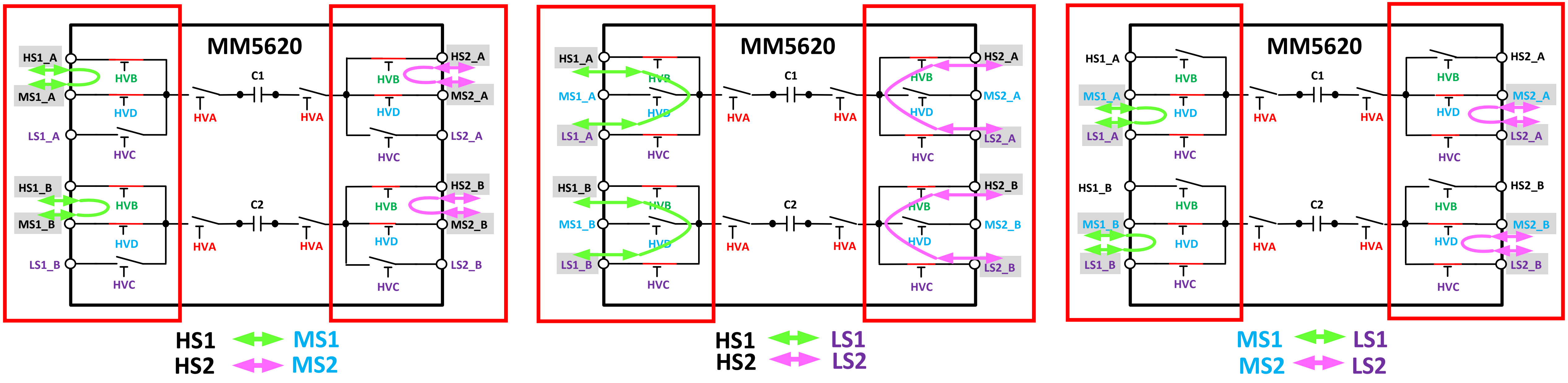


LS1 ↔ LS2

Case 3

MM5620/MM5622 – Six Signal Paths

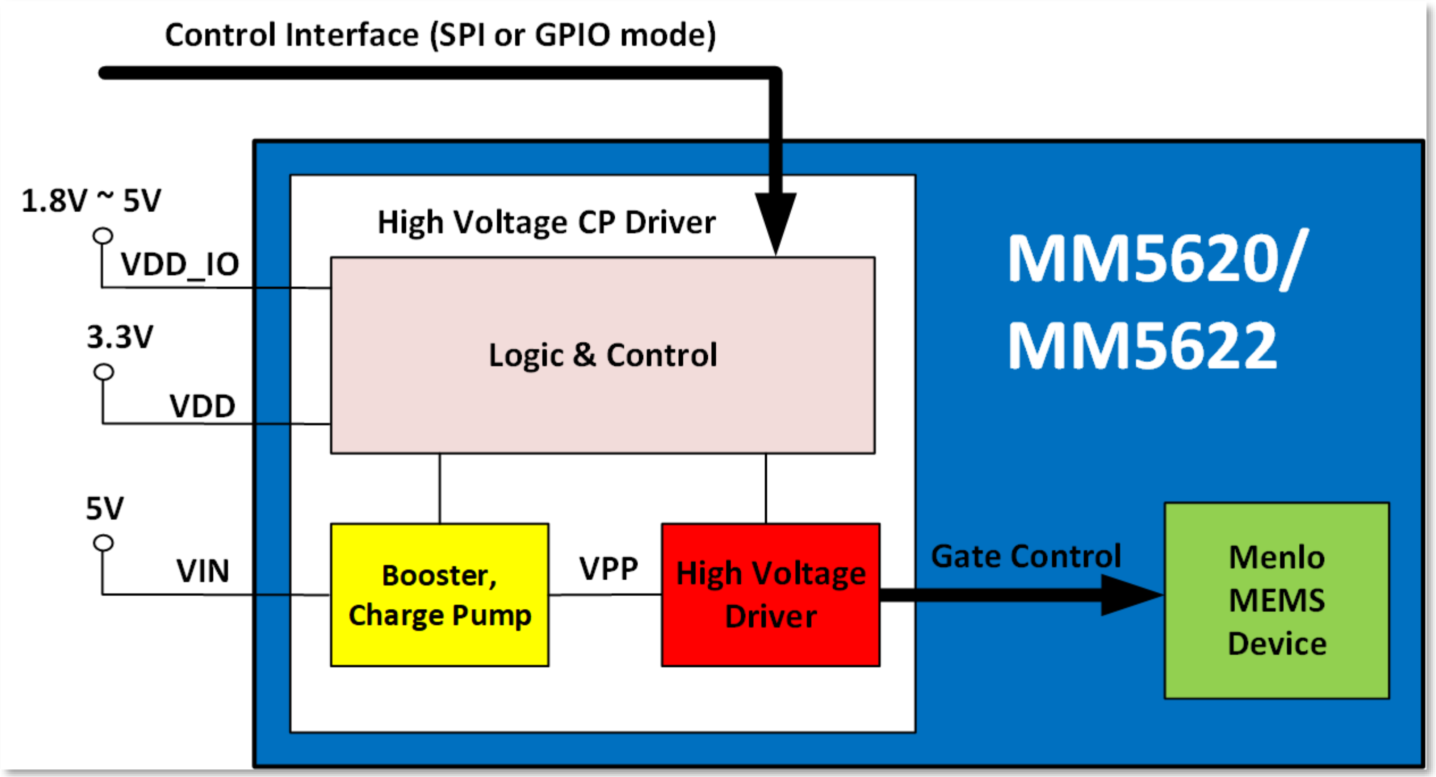
- Additional three DC-coupled signal paths for the MM5620
- The same DC-coupled signal paths supported for the MM5622 device
  - Case 4: High Speed 1 to Medium Speed 1 and High Speed 2 to Medium Speed 2
  - Case 5: High Speed 1 to Low Speed 1 and High Speed 2 to Low Speed 2
  - Case 6: Medium Speed 1 to Low Speed 1 and Medium Speed 2 to Low Speed 2



Case 4 **Case 5** **Case 6**

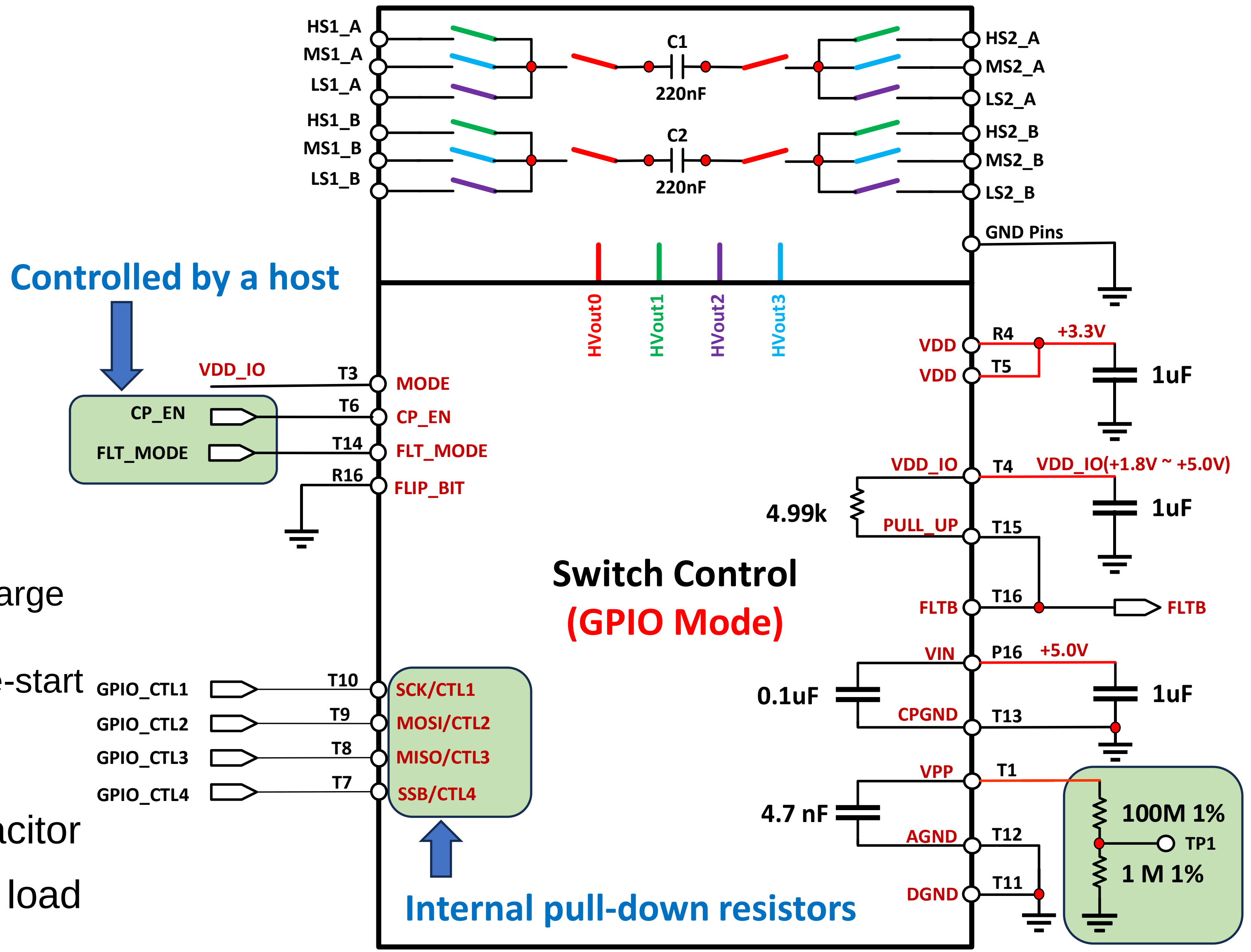
MM5620/MM5622 - MEMS Switch Control Block Diagram

- The communication interface: GPIO and SPI
- VDD_IO: Digital I/O supply (+1.8V to +5.0V)
- VDD: +3.3V supply to analog circuits
- VIN: +5V supply to the internal charge pump
- Should not need to sequence the power supplies



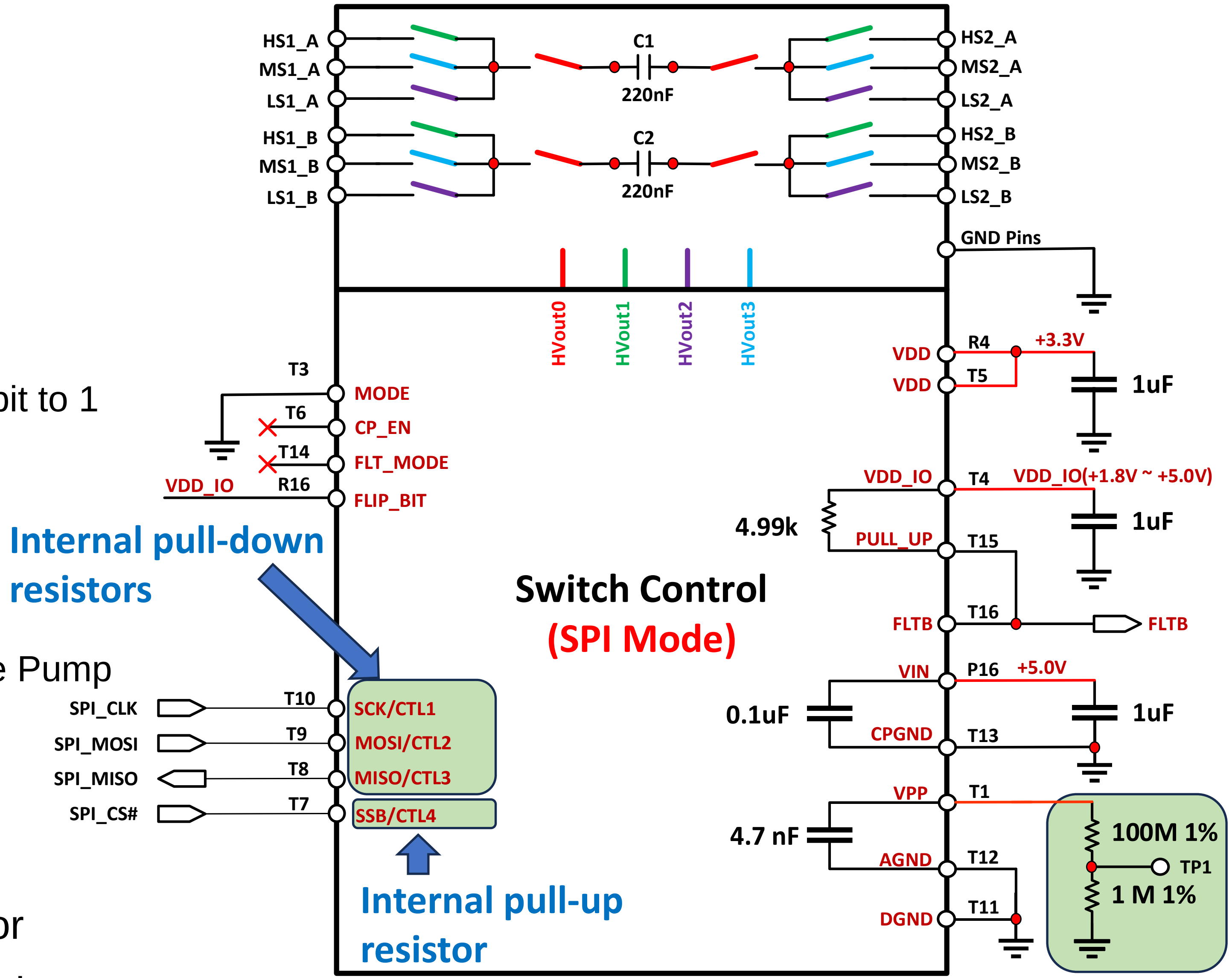
MM5620/MM5622 – External Circuit for GPIO Mode

- Enable the GPIO Mode:
  - MODE: Connect to VDD_IO
  - FLIP_BIT: Connect to GND
- Enable the Charge Pump
  - CP_EN: Connect to VDD_IO
- Disable the Fault Mode:
  - FLT_MODE: Connect to VDD_IO
  - Monitoring VDD and VPP when enabled
- FLTB:
  - Fault indicator
  - Open-Drain output
  - Goes low when the fault is detected & the Charge Pump is turned off.
  - Toggle the CP_EN pin low and then high to re-start the IC
  - Can be left open if not used
- Bypass with a low ESR 1 µF ceramic capacitor
- VPP can be probed with a high resistance load



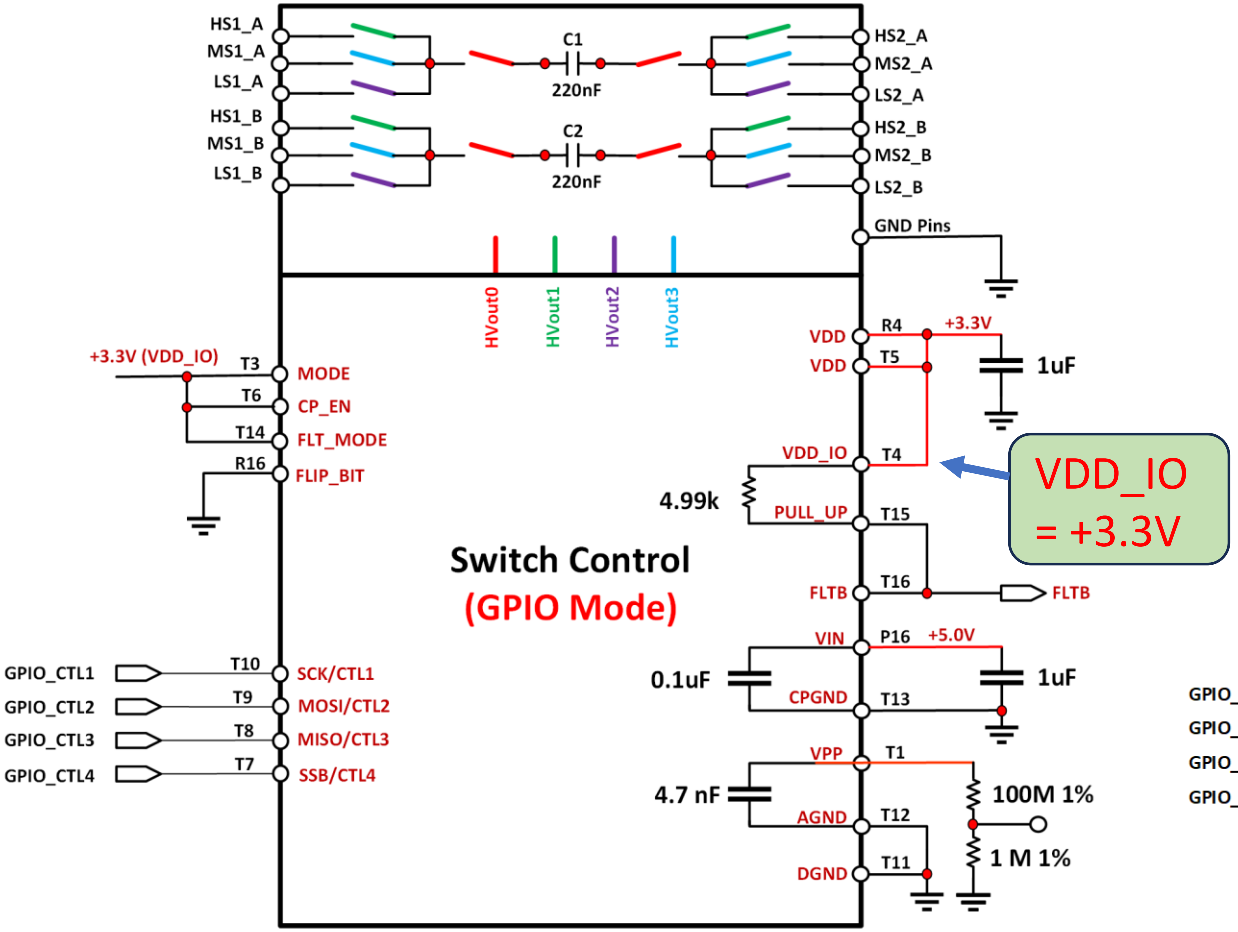
MM5620/MM5622 – External Circuit for SPI Mode

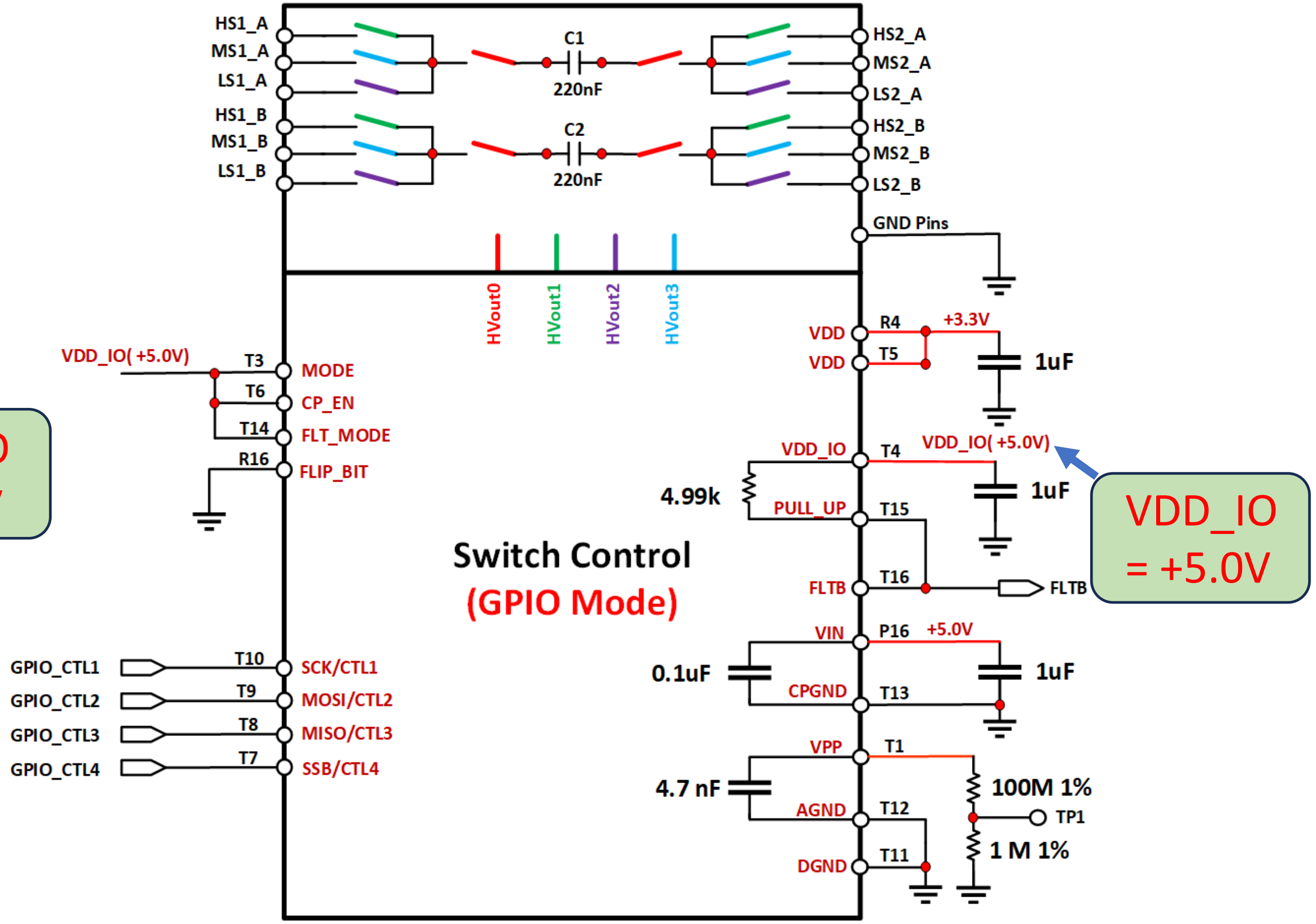
- Enable the SPI Mode:
  - MODE: Connect to GND
- Enable Spread Spectrum:
  - FLIP_BIT: Connect to VDD_IO
- Enable the Charge Pump
  - CP_EN pin: No connect, set the CPEN bit to 1
- Disable the Fault Mode:
  - FLT_MODE pin: No connect, Set the FLTMODE bit to 1
  - Monitoring VDD and VPP when enabled
- FLTB:
  - Fault indicator
  - Open-Drain output
  - Goes low when the fault is detected & the Charge Pump is turned off.
  - Toggle the CPEN bit low and then high to re-start the IC
  - Can be left open if not used
- Bypass with a low ESR 1 µF ceramic capacitor
- VPP can be probed with a high resistance load



MM5620/MM5622 – External Circuit for GPIO Mode

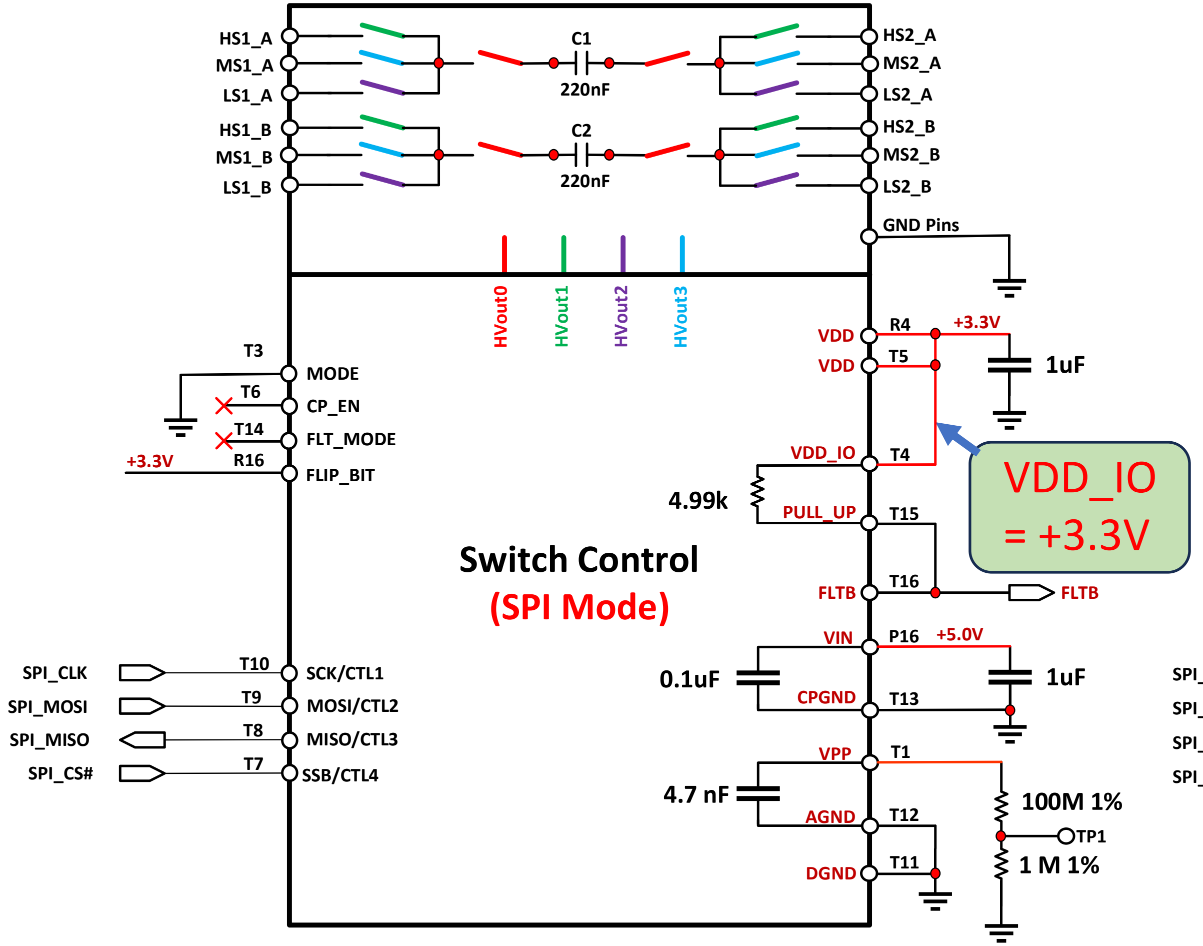
- The Charge Pump is enabled after POR
- The Fault Mode is disabled after POR

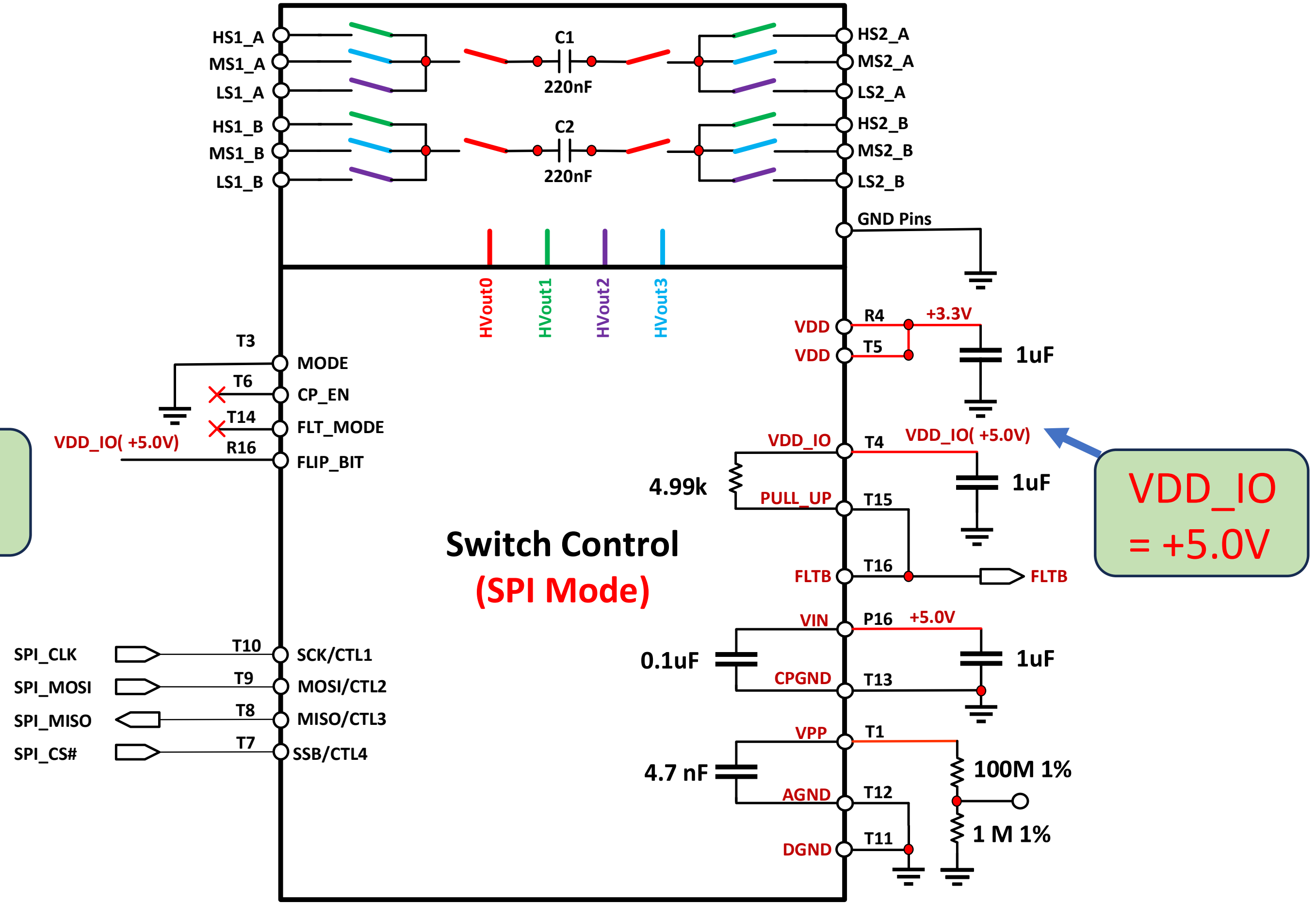




MM5620/MM5622 – External Circuit for SPI Mode

- The Charge Pump needs to be enabled by setting the CPEN bit = 1 in SPI mode
- The Fault Mode can be deactivated by setting FLT_MODE bit = 1 in SPI mode





MM5620 – Measured S-Parameter Performance

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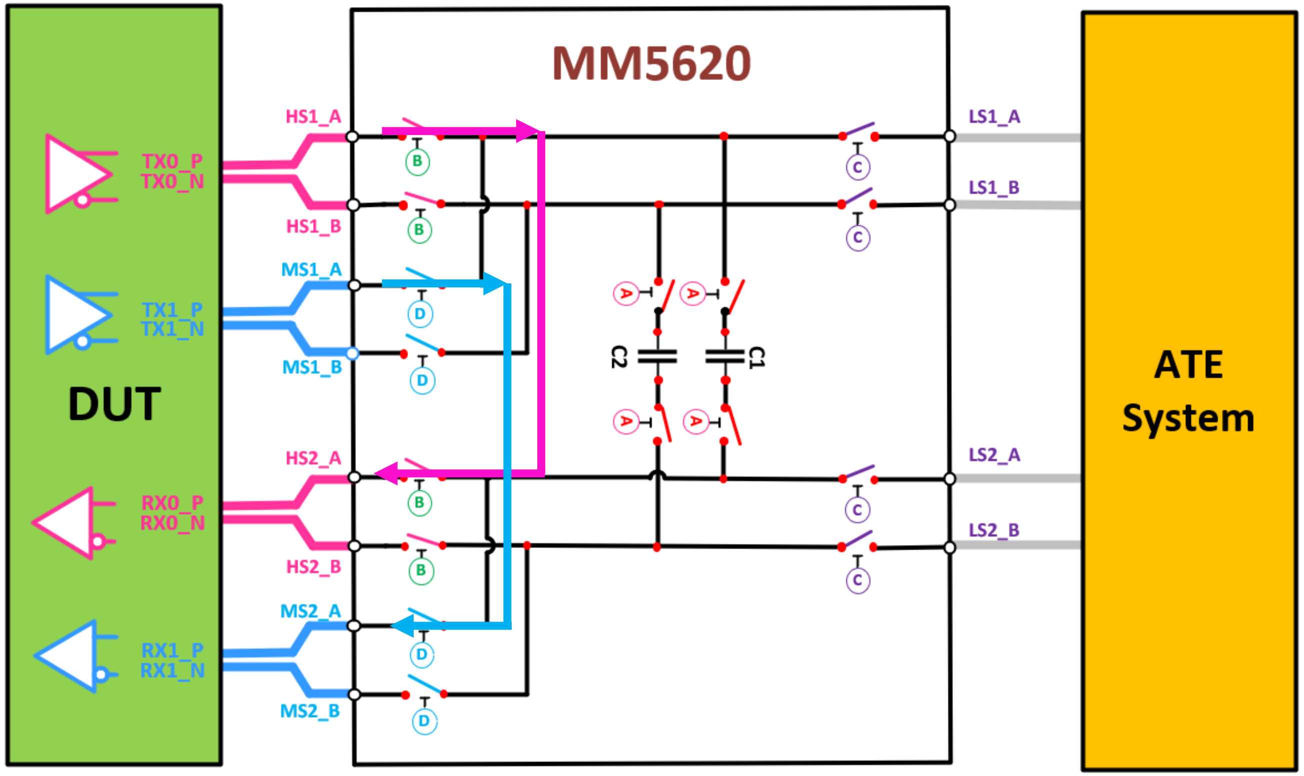
Parameter	Symbol	Typical	Unit	Conditions
Differential Insertion Loss				
High Speed (HS1 to HS2)	**SDD21**	**1.5**	dB	@16GHz, De-embedded
Medium Speed 2(MS1 to MS2)		**2.0**		
HS1 to MS1		**1.4**		
HS2 to MS2		**1.4**		
HS1-LS1		**2.9**		@ 6 GHz, Not de-embedded
HS2-LS2		**2.9**		
MS1_LS1		**3.1**		
MS2_LS2		**3.1**		
Low Speed (LS1 to LS2)		**3.0**		@ 3 GHz, Not de-embedded
Differential Return Loss				
High Speed (HS1 to HS2)	**SDD11**	**28**	dB	@16GHz, De-embedded
Medium Speed 2(MS1 to MS2)		**23**		
HS1 to MS1		**13**		
HS2 to MS2		**12**		
HS1-LS1		**23**		@ 6 GHz, Not de-embedded
HS2-LS2		**23**		
MS1_LS1		**25**		
MS2_LS2		**25**		
Low Speed (LS1 to LS2)		**27**		@ 3 GHz, Not de-embedded

MM5622 – Measured S-Parameter Performance

Parameter	Symbol	Typical	Unit	Conditions
Differential Insertion Loss				
High Speed (HS1 to HS2)	**SDD21**	**1.1**	dB	@16GHz, De-embedded
Medium Speed 2(MS1 to MS2)		**1.6**		
HS1 to MS1		**1.4**		
HS2 to MS2		**1.4**		
HS1-LS1		**2.9**		@ 6 GHz, Not de-embedded
HS2-LS2		**2.9**		
MS1_LS1		**3.1**		
MS2_LS2		**3.1**		
Low Speed (LS1 to LS2)		**1.5**		@ 9 GHz, De-embedded
Differential Return Loss				
High Speed (HS1 to HS2)	**SDD11**	**29**	dB	@16GHz, De-embedded
Medium Speed 2(MS1 to MS2)		**28**		
HS1 to MS1		**12**		
HS2 to MS2		**10**		
HS1-LS1		**23**		@ 6 GHz, Not de-embedded
HS2-LS2		**23**		
MS1_LS1		**25**		
MS2_LS2		**25**		
Low Speed (LS1 to LS2)		**10**		@ 9 GHz, De-embedded

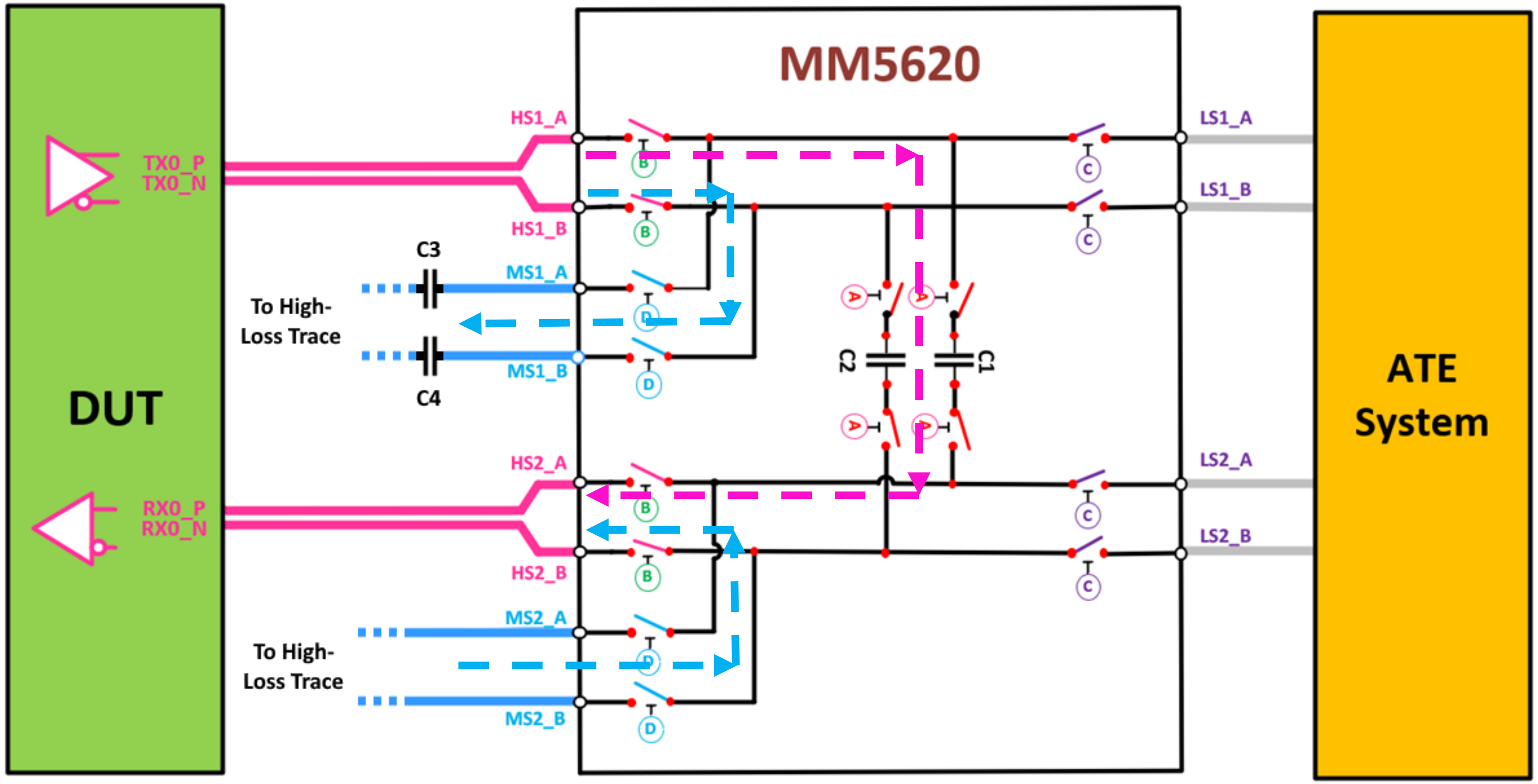
MM5620 – Double Density HSIO Loopback Mode Test

- Test Two PCIe 5/6 lanes at high-speed using ONE MM5620 device
  - TX0_X ← → RX0_X (HS1 ← → HS2) at speed test
  - TX1_X ← → RX1_X (MS1 ← → MS2) at speed test
- LS signals can be shared for low frequency and DC sweep test
- Two transmitters can be ALWAYS ON to reduce test time
- Fully bi-directional signal paths



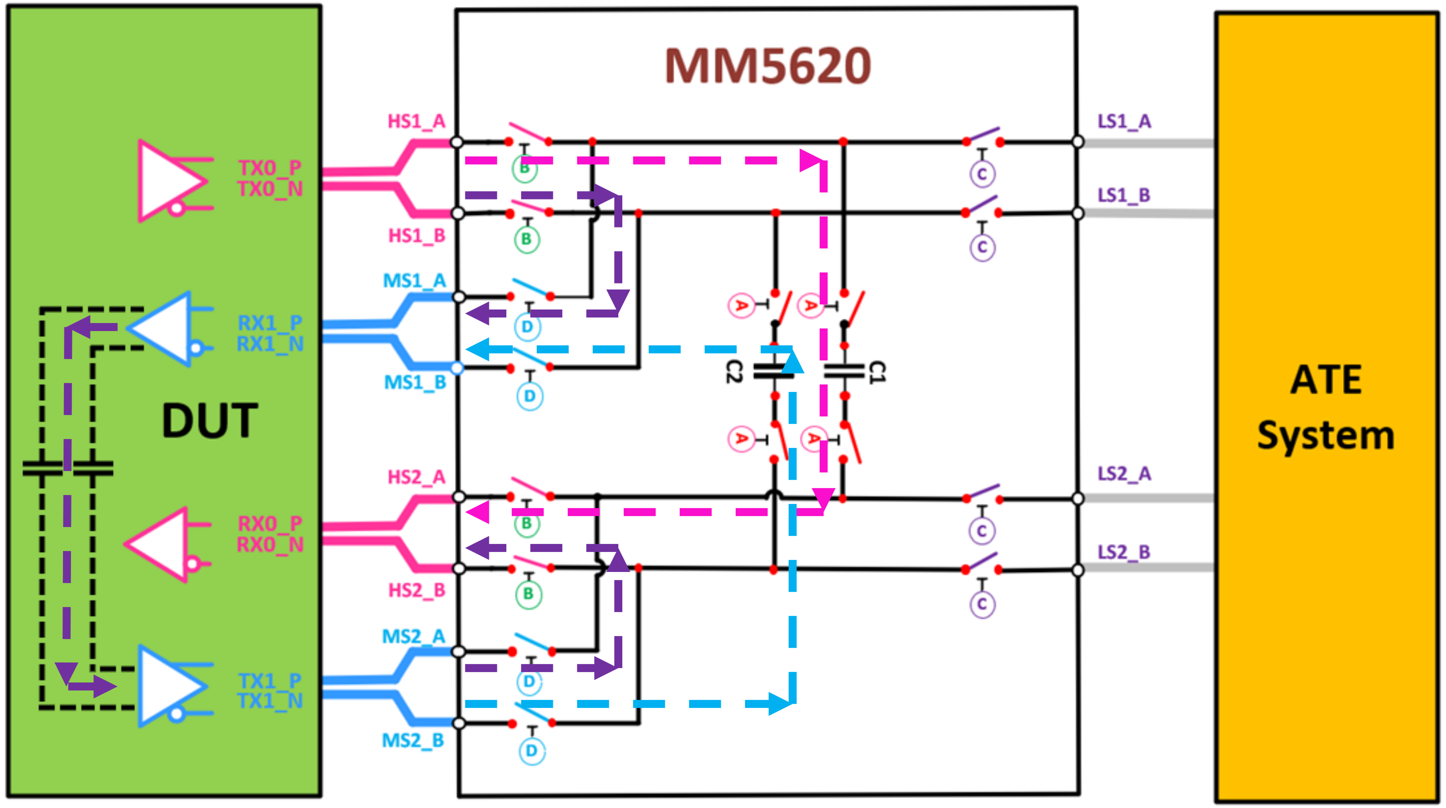
MM5620 – Low-Loss + High-Loss Loopback Test

- Test one PCIe 5/6 lane at high-speed using one MM5620 device
  - HS1 ← → HS2 (through internal caps) for low-loss loopback test
  - HS1 ← → MS1 ← EXTERNAL → MS2 ← → HS2 for high-loss loopback test, to simulate backplane losses
- HS1 ← → LS1, HS2 ← → LS2 signals used for low frequency and DC sweep test
- Fully bi-directional signal paths



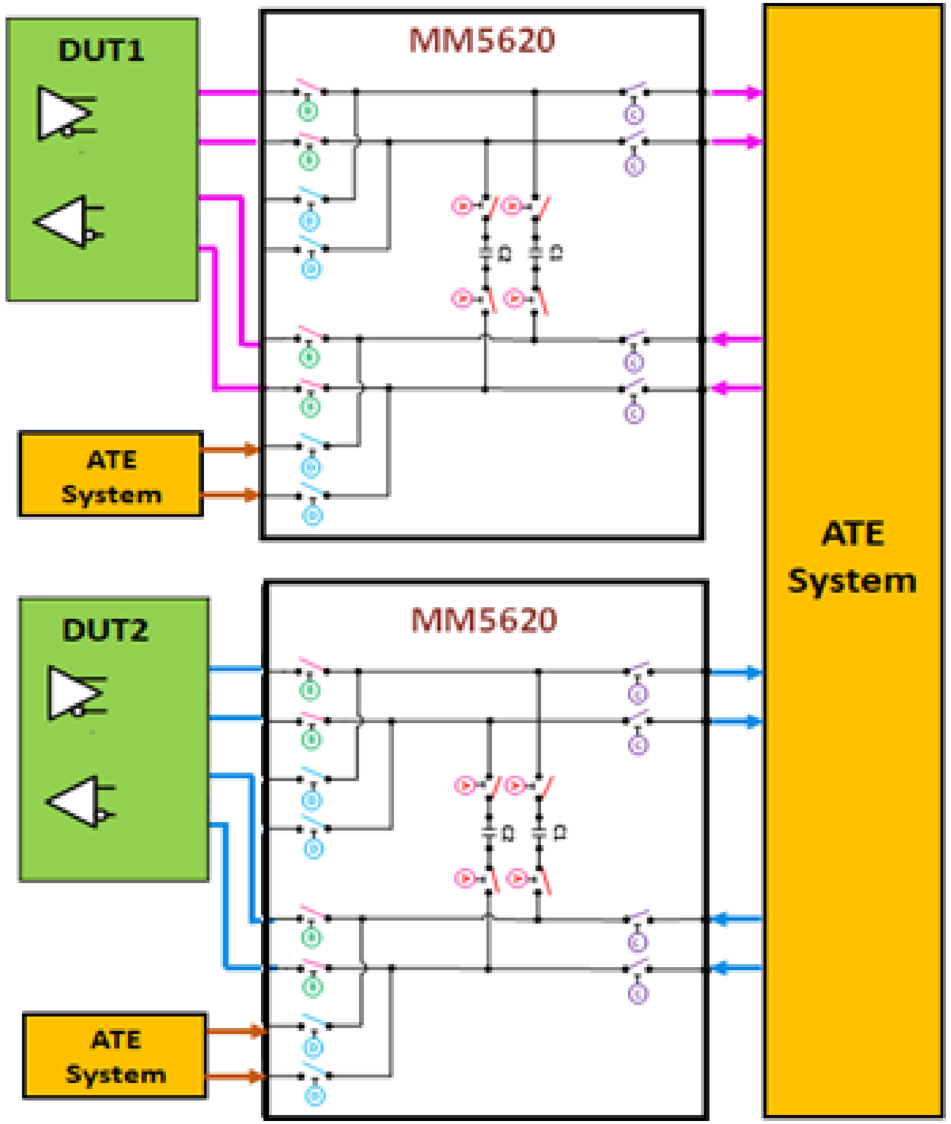
MM5620 – Double Density Low Loss + High-Loss Loopback Test

- Test TWO PCIe 5/6 lanes for low-loss loopback, AND one high-loss loopback, using ONE MM5620 device
  - HS1 ← → HS2 low-loss loopback test
  - MS1 ← → MS2 low-loss loopback test
  - HS1 ← → MS1 ← DUT → MS2 ← → HS2 high-loss loopback test
- LS signals can be shared for low frequency and DC sweep test
- **Requires loopback path with AC coupling internal to DUT**

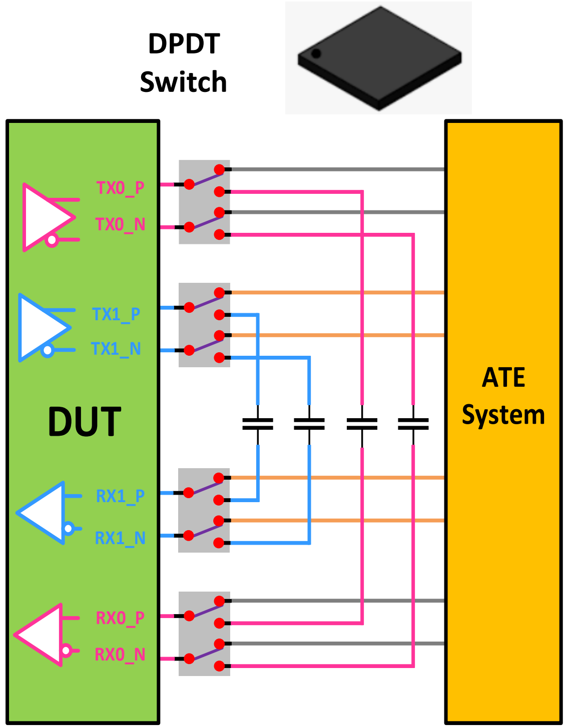


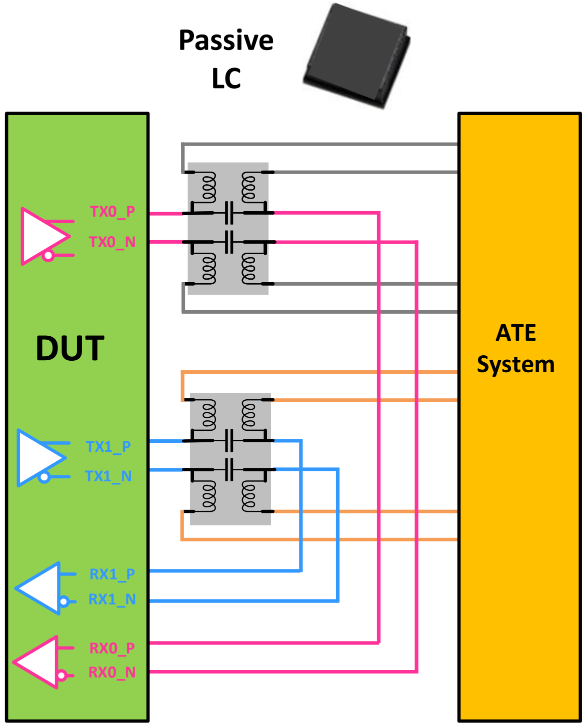
MM5620 – Double Density HSIO Loopback Test Applications

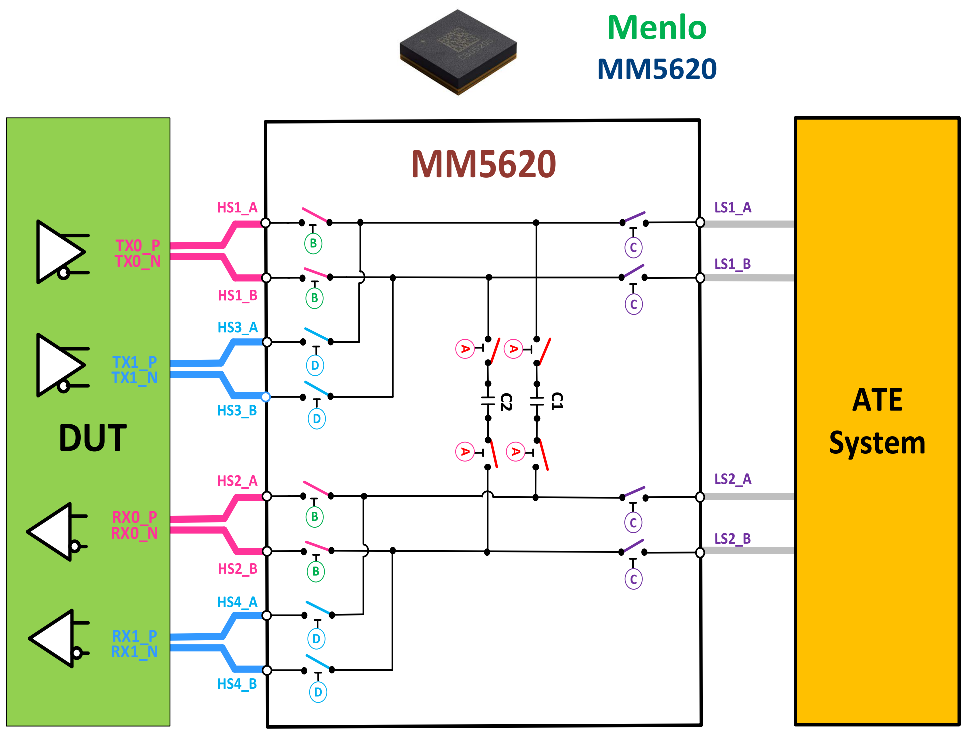
- Utilizing two MM5620 differential switches configured in a dual DPDT configuration with parallel loopback and ATE tests
- Supports 64 Gbps data rates to meet the latest PCIe Gen 6 requirements
- Real time double density parallel tests to reduce testing cost



MM5620 – Application Benefits for Automated SoC Testing







Metrics	Parameters	DPDT Switch	Passive LC	Menlo MM5620
Performance	Loopback Channel Data Rate	★★ 64 Gbps (PAM4)	★★★★ 128 Gbps (datasheet)	★★★ 64 Gbps (PAM4)
	ATE Test Channel Frequency Range (3dB)	★★★ DC to 18 GHz	★ DC to <100 MHz	★★★★ DC to 20 GHz
Versatility	Transmitters Sharing a Receiver	★ No (need external switches)	★ No (need external switches)	★★★★ Yes
	Loopback-ATE Channel Isolation	★★★★ 13 dB (18 GHz)	★★ By inductor (low ISO for <200 MHz)	★★★★ 50 dB (18 GHz)
Board Density	BOM Count	★ 4x switches, 4x caps	★★★ 2x LC chips	★★★★ 1x MM5620
	Footprint	★★ Four 5mm x 4mm	★★★★ Two 4.3mm x 4mm	★★★ One 8.2mm x 8.2mm

Data from suppliers' online datasheet, subject to change and verification, scoring based on specs comparison

MM5620 vs Relay Supplier – Switch Replacement Cost Savings

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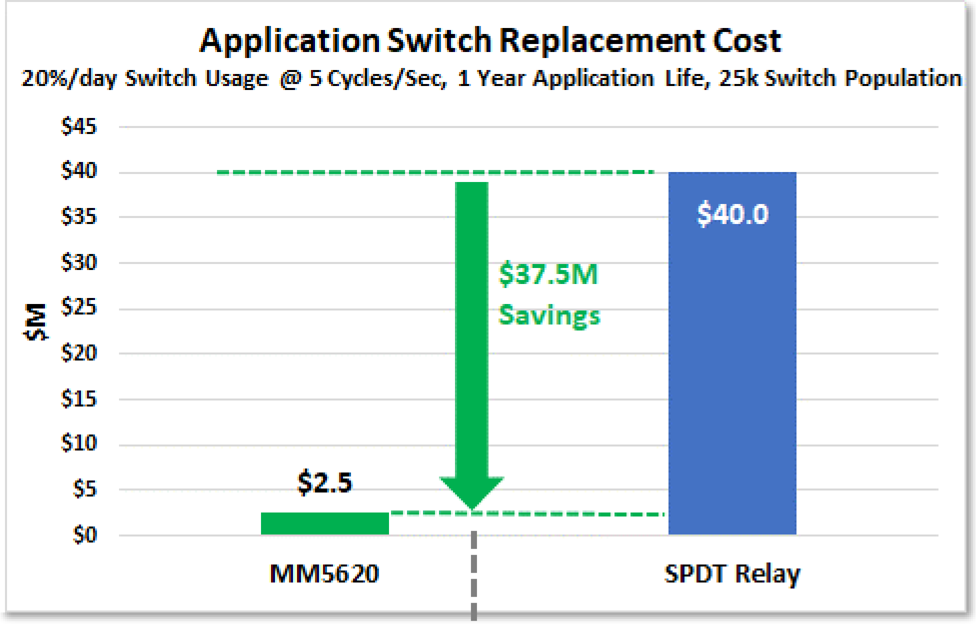
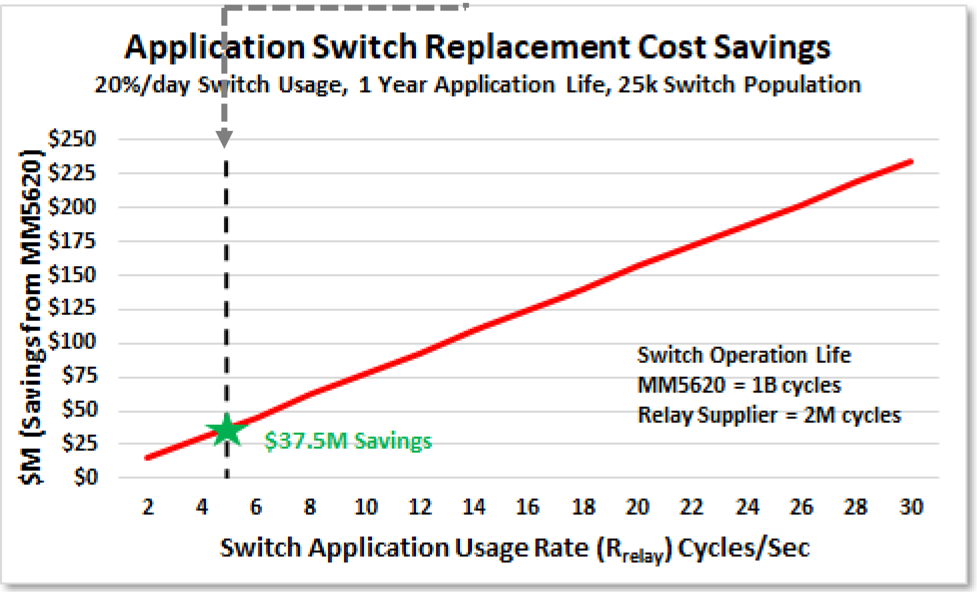
Application Switch Replacement Cost Savings Illustration Accumulated from Switch Operating Life over Application Life

Application Switch Replacement Cost of Ownership *Green = inputs*	Symbol	Calculation	Unit	MM5620	Relay Supplier
Switch operation life	L_{switch}	*Datasheet*	*Mcycles*	1,000	2
Application switch usage cycle rate	R_{switch}	*Estimates for illustration*	*cycles/sec*	5	5
Application switch usage % per day (24/7 = 100%)	D_{switch}	*Estimates for illustration*	*%*	20%	20%
Switch usage life	T_{RL}	$= (L_{switch}/R_{switch})/D_{switch}$	*years*	31.7	0.1
Total switch usage cycles per year	U_{switch}	$= L_{switch}/T_{RL}$	*Mcycles/yr*	32	32
Application life	T_{AL}	*Estimates for illustration*	*years*	1.0	1.0
Switch replacement cycles over apps life	$N_{replace}$	$= T_{AL}/T_{RL}$	*#*	1	16
Application switch population	N_{switch}	*Estimates for illustration*	*#*	25,000	25,000
Switch unit cost	$\$P_{switch}$	*Estimates for illustration**	*$*	$100	$100
Switch replacement cost	$\$_{replace}$	$= N_{replace} \times N_{switch} \times \$P_{switch}$	*$*	$2,500,000	$40,000,000
Switch cost savings (relative to MM5620)	$\$_{savings}$	$= \$_{replace} - \$_{replace\_MM1205}$	**$**	--	**$37,500,000**

*Switch unit cost for illustration only, DOES NOT imply actual cost for MM5620 and relay supplier

- Switch operating life: 1B (MM5620/MM5622) 2M (Relay Supplier)
- Application life: 1 year, 25k switch population, $100/switch*
- Application switch usage rate: 5 cycles/sec (18k cycles/hr)
- Application usage per day: 20%
- Savings will be HIGHER when:
  - Switch usage rate and/or application daily usage % is higher
  - Supplier x switch operating life is shorter and/or switch cost is higher
  - Application life is longer
  - Switch population is larger





MM5620 S-Parameter Performance (HS1 to HS2 Signal Path)

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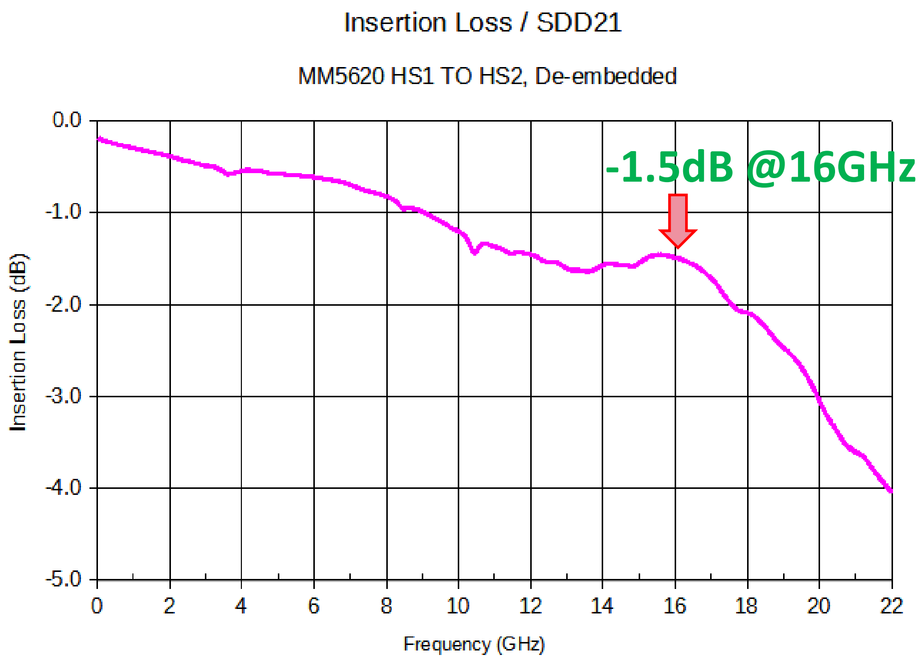
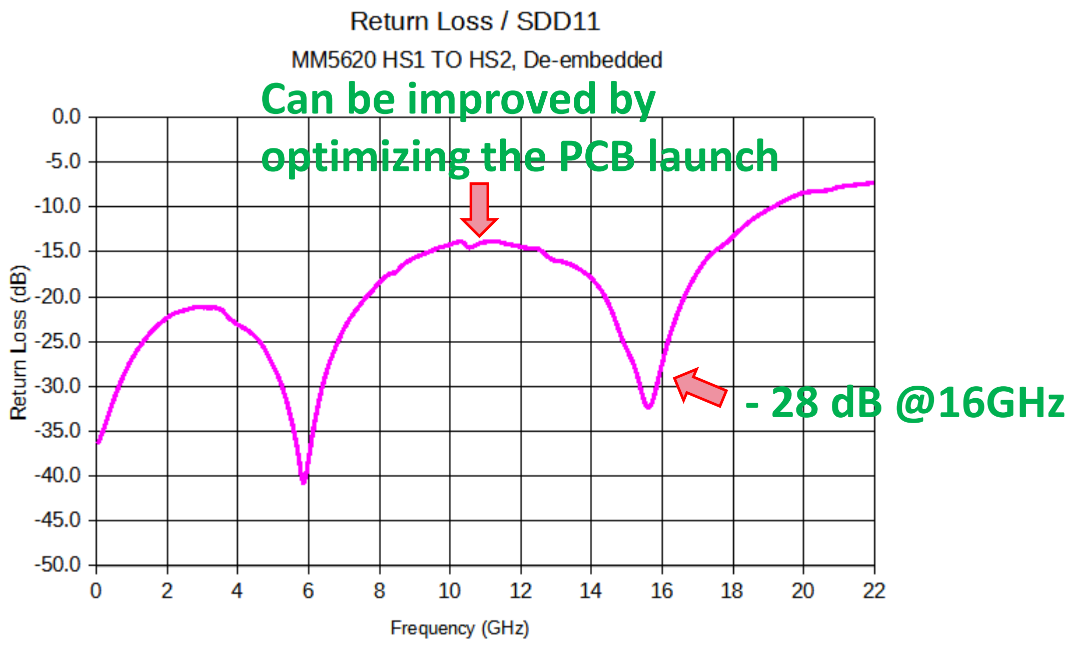
Frequency Domain Analysis

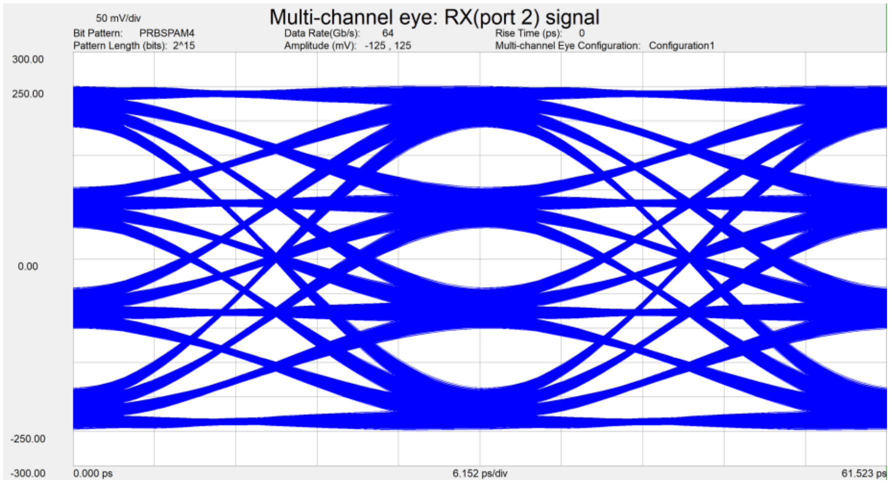




Time Domain Analysis

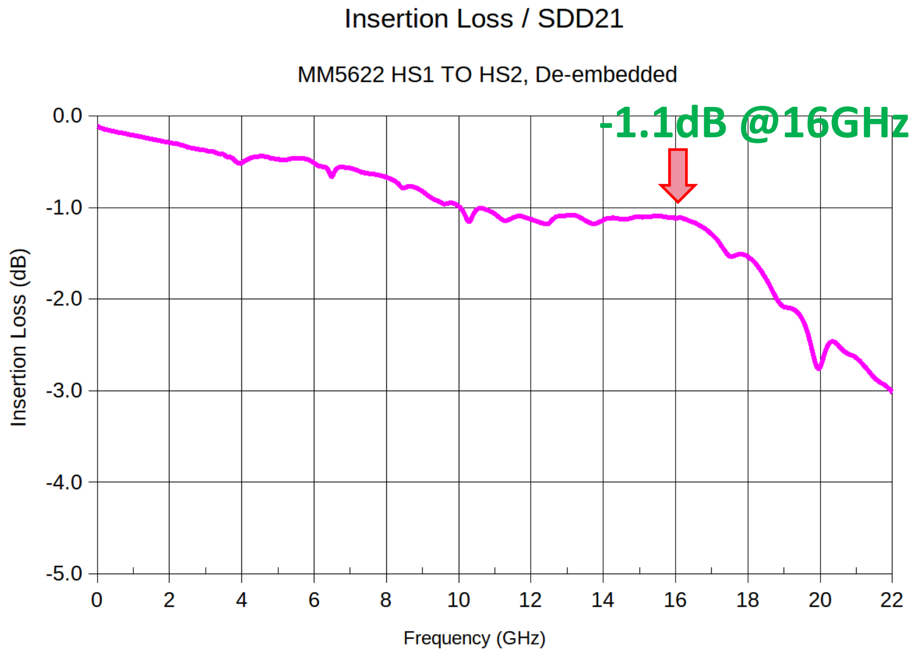
Eye-Diagram Test Conditions

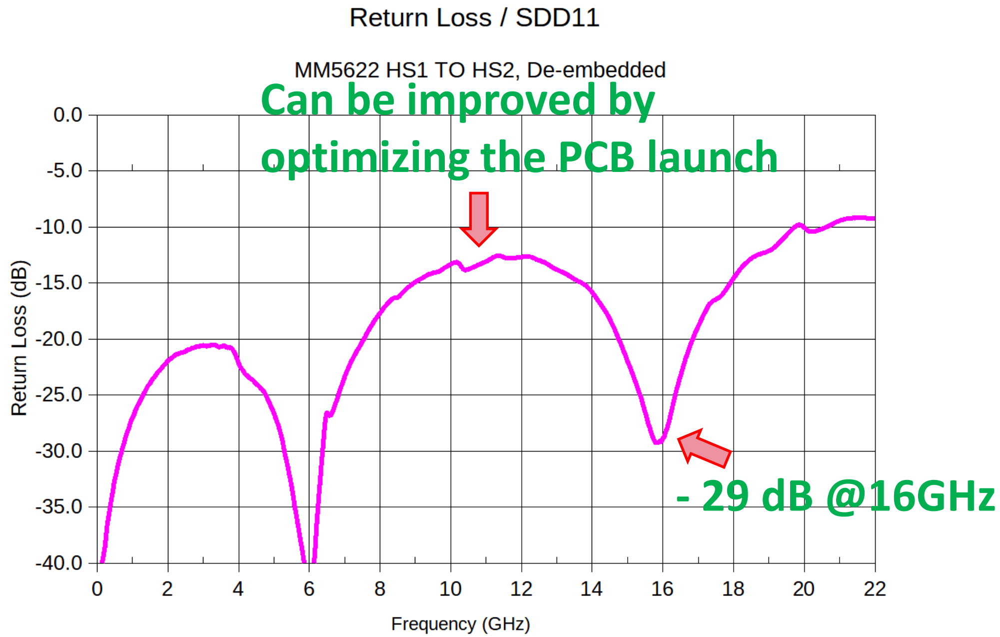
- PCIe Gen6
- PAM4, 32 Gbaud (64Gbps), PRBS 2^{15}-1
- 500mVpp (+250 mV/-250mV)



MM5622 S-Parameter Performance (HS1 to HS2 Signal Path)

Frequency Domain Analysis





Time Domain Analysis

Eye-Diagram Test Conditions

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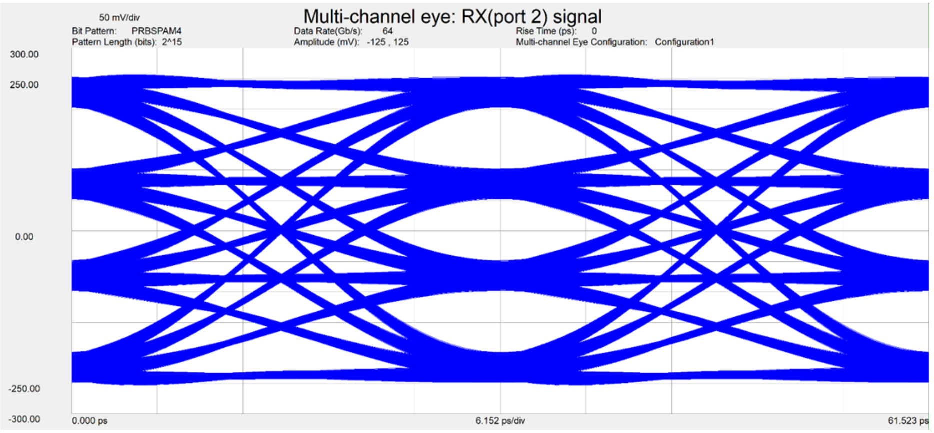


MM5620/MM5622 – Customer Evaluation Board R.4.0

- EVK performance is improved with optimized PCB launch
- Return loss is better than -18dB across frequencies up to 16GHz

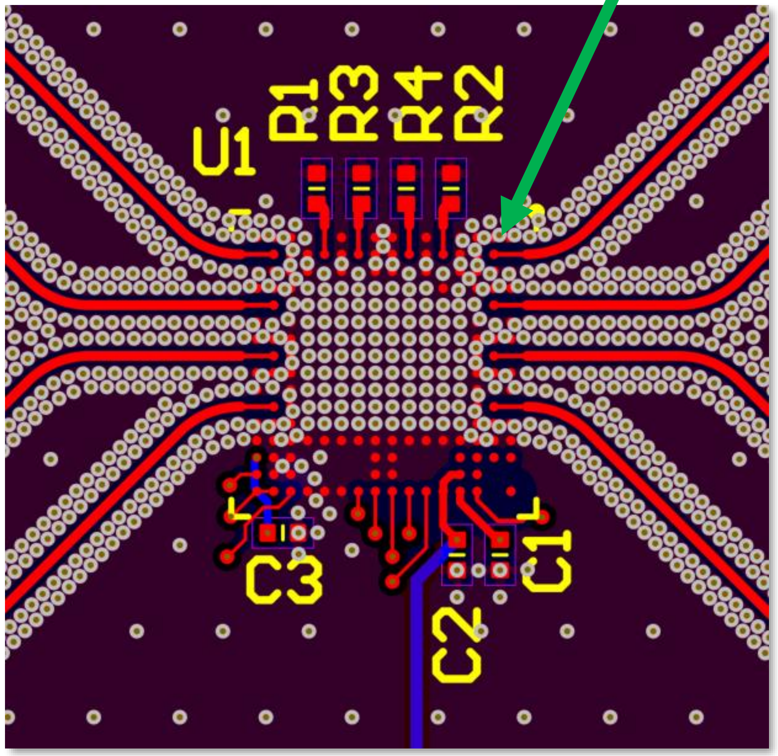
Neck-down trace

MS1A

HS1A

HS1B

MS1B



MS2A

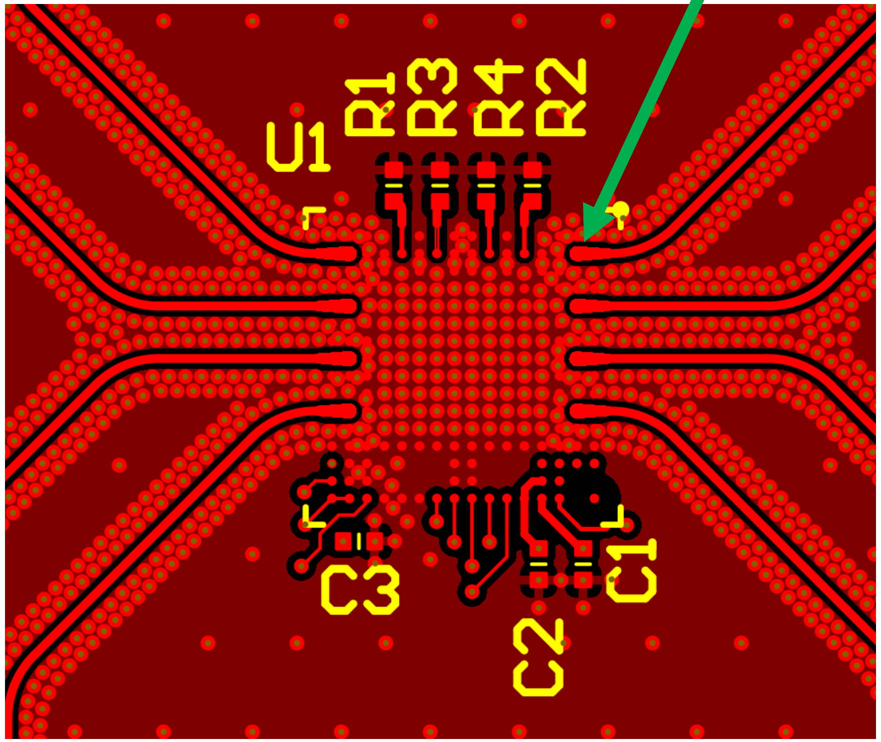
HS2A

HS2B

MS2B

MM5620 EVK1 R1.0

Teardrop trace



MM5620 EVK1 R2.0

High-Speed Digital PCB Design

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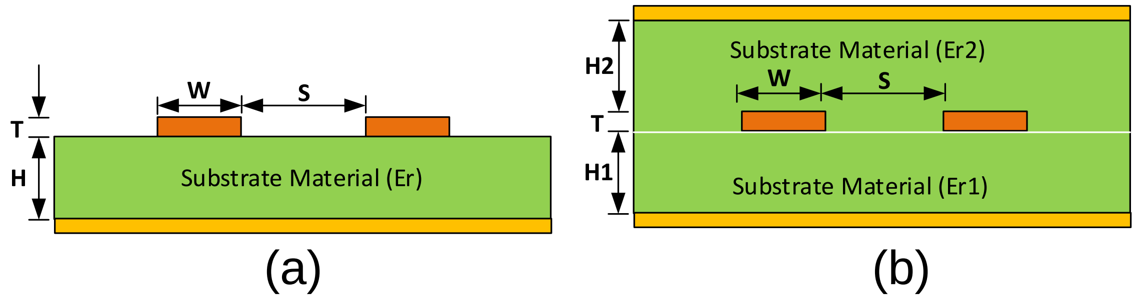
- Need to get deep understanding of your fabrication houses' capability and details of their design rules in advance, then work very closely together with them.
- Most high-speed differential lines use either an edge-coupled microstrip or an edge-coupled stripline.



T(Copper Thickness), W(Trace Width), S (Spacing), H (Substrate Height), and B (Substrate height) (a) edge-coupled microstrip (b) edge-coupled stripline

- Use better dielectric material with low dielectric constant, low-loss tangent, better surface roughness, Reverse Treated Copper Foil
- Use better PCB finish (plating method) such as EPIG, ISIG, ENEPIG, etc. if the design has high-speed routing on top/bottom layer.

High-Speed Digital PCB Design

- To optimize transmission line design, wider and shorter traces are better to minimize the insertion loss.
- For the differential signals, routing should be smooth with minimum bends and tight length matching is required.
- To provide a proper de-embedding, the 2x-through needs to be implemented with symmetrical routing and placement.
- Stitching vias are required to be placed along all the high-speed routing from DUT to Connectors. If space allows, it is ideal to implement two rows of stitching vias along the RF signals routing.
- Optimizing via transitions is necessary to minimize the impedance mismatch. A TDR simulation using 3D EM tools is a good method to check the impedance of vias and optimize it.
- Solder mask needs to be removed on high-speed traces.
- Although it takes additional time, confirmation by running post-layout full 3D EM simulation, to obtain S-parameter, TDR, and eye diagram results, is a must to ensure that the board layout can meet the requirements.

Selecting The Right RF Connector

- The Nyquist frequency is 16GHz for both PCIe Gen5 and Gen6; for digital signal, need to use at least K connector (2.92mm, up to 40GHz) or V connector (1.85mm, up to 67GHz).
- For high-speed, high performance RF board, it is recommended to use a solderless PCB connector as shown in Figure below.
- For the edge launch connector, copper underneath of the connector should be flushed with the board edge, otherwise the signal will lose reference and will get an inductive spike from that area which will affect performance.

(a) Edge Launch Connector(2.92mm/2.4mm)

(b) solderless PCB connectors – 45 degree (2.92mm/1.85mm)

MM5620/MM5622 SPI Control

Daisy Chain Control Example

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Control Register Definition

Control Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
WR_EN	FSTAT	SLEEP	FLTMODE	VPPCOMP	X	CPEN	X
bit 15							bit 8
1	0	0	1	0	0	1	0

Bit 15: WR_EN
"1" :Write Control
"0" : Read Control

Bit 13: SLEEP
"1" : Enabled
"0" : Disabled

Bit 13:
"1" : VPP under-voltage comparator is disabled
"0" : VPP under-voltage comparator is enabled

Bit 14: FSTAT
"1" : Faulted
"0" : Not faulted

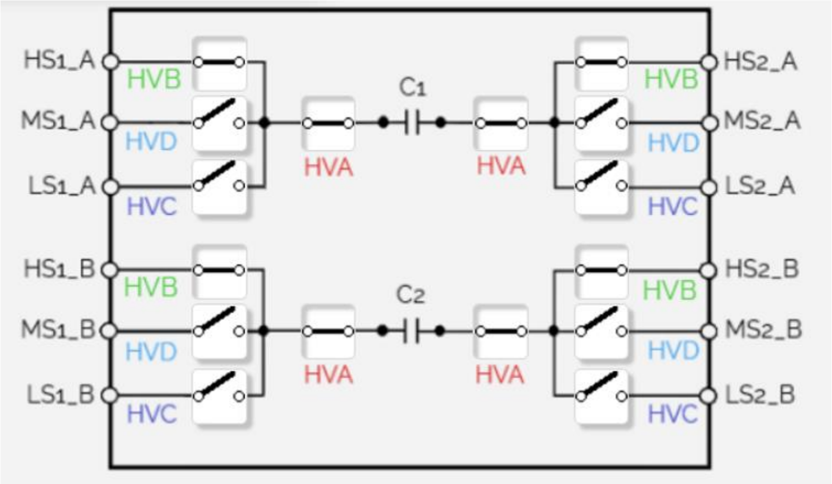
Bit 12: FLTMODE
"1" : Fault Detection Disabled
"0" : Fault Detection Enabled

Bit 9: CPEN
"1" : Charge Pump Enabled
"0" : Charge Pump Disabled

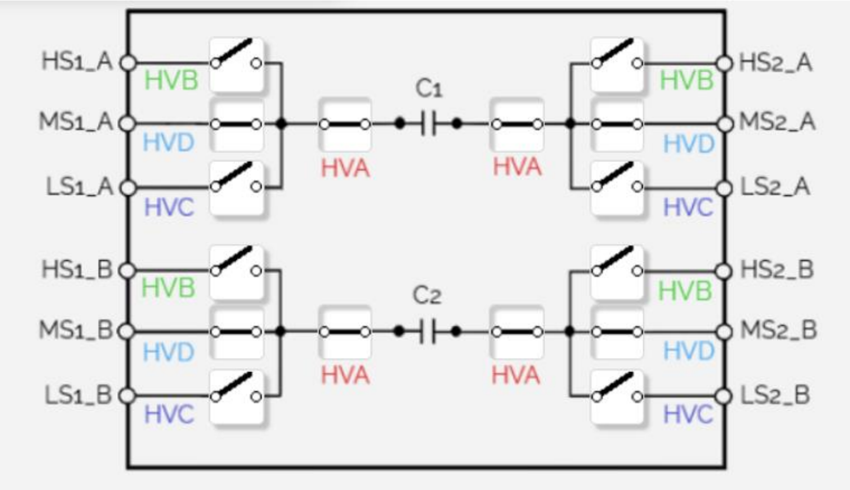
Status Register Definition

State Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
0	0	0	0	**HVD**	**HVC**	**HVB**	**HVA**
bit7							bit 0
0	0	0	0	1	0	0	1
0	0	0	0	0	0	1	1



HS1 to HS2 Path: HVA and HVB ON(0x03)

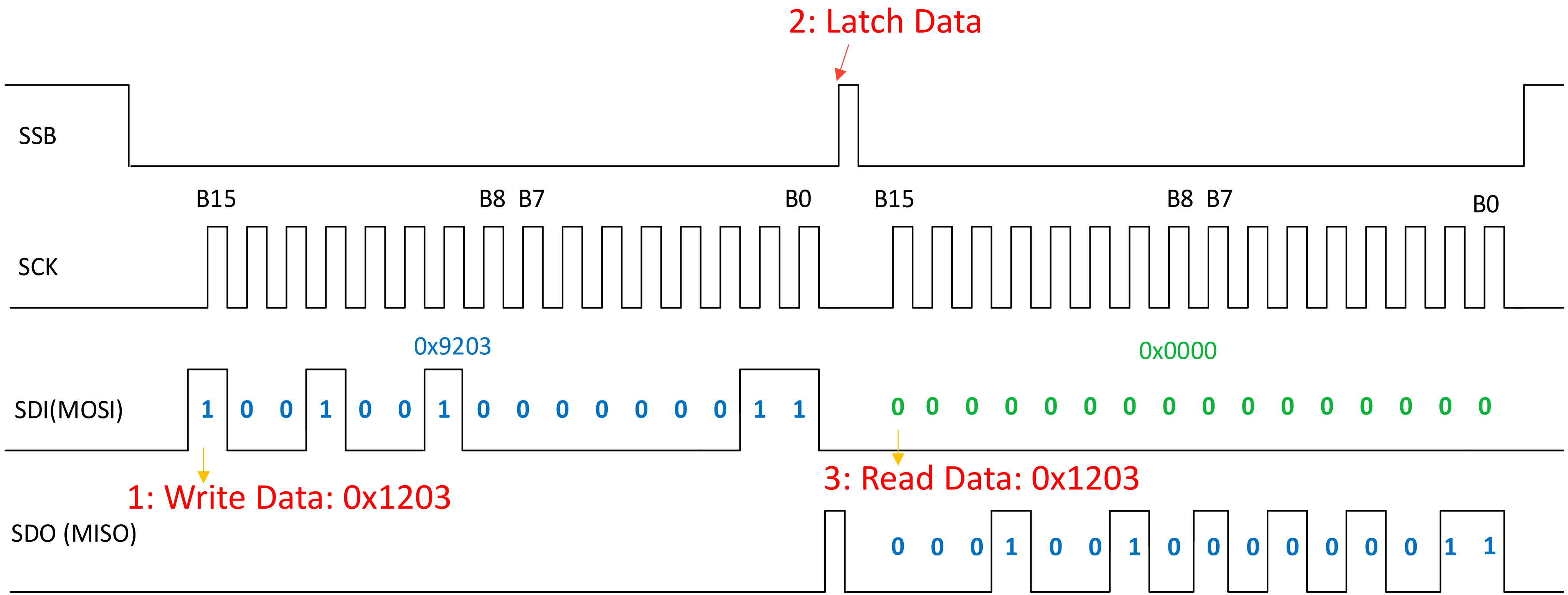


MS1 to MS2 Path : HVA and HVD ON (0x09)

Control Patterns

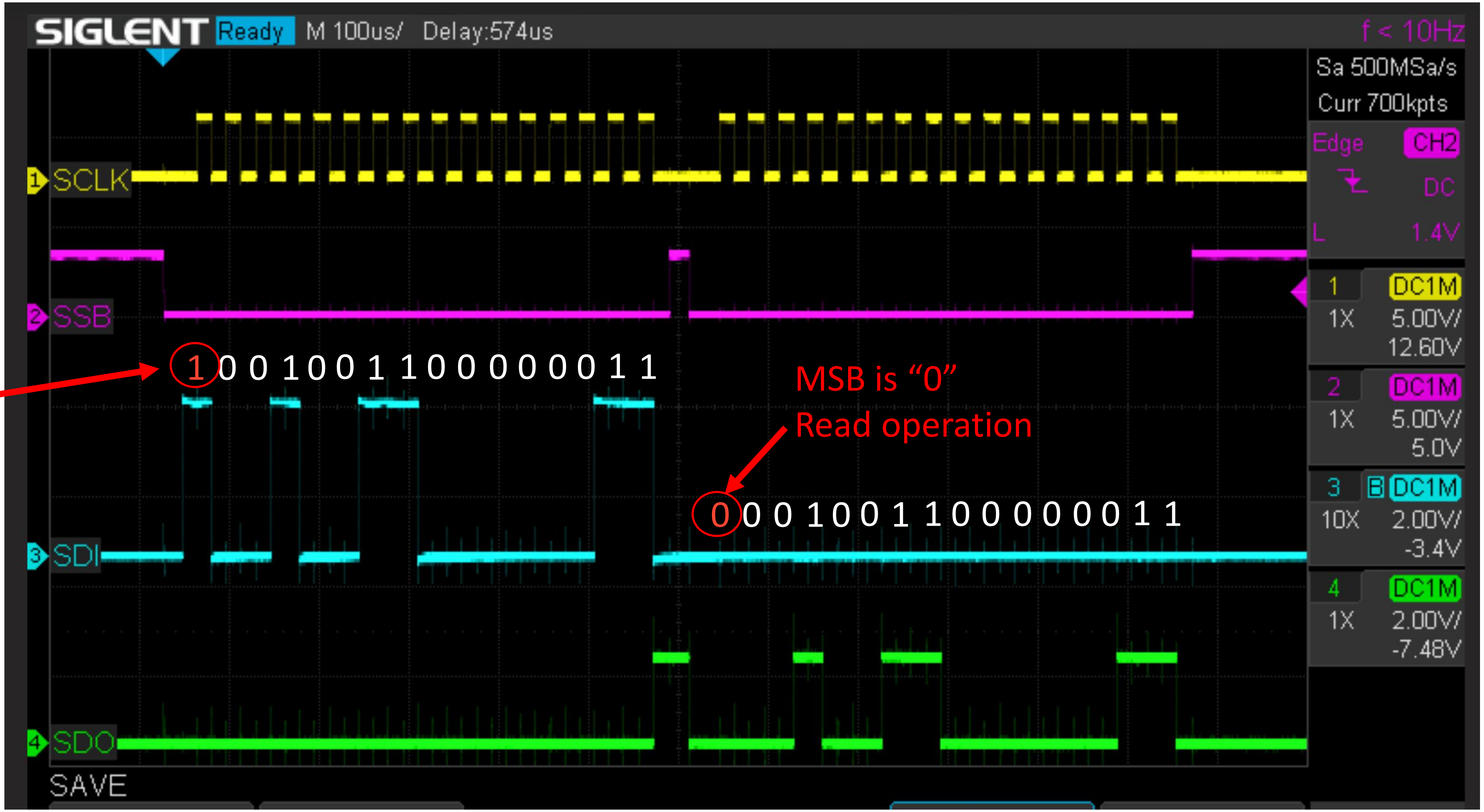
Control Example (one 16-bit word)	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0x00 00 – READ DATA	0				0				0				0			
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x92 00 – Charge Pump ON, Fault Mode DISABLE, ALL OFF (OPEN)	9				2				0				0			
	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
0x92 03 – Charge Pump ON, Fault Mode DISABLE, HS1 – HS2	9				2				0				3			
	1	0	0	1	0	0	1	0	0	0	0	0	0	0	1	1
0x92 05 – Charge Pump ON, Fault Mode DISABLE, LS1 – LS2	9				2				0				5			
	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	1
0x92 06 – Charge Pump ON, Fault Mode DISABLE, HS1 – LS1 and HS2 – LS2	9				2				0				6			
	1	0	0	1	0	0	1	0	0	0	0	0	0	1	1	0
0x92 09 – Charge Pump ON, Fault Mode DISABLE, MS1 – MS2	9				2				0				9			
	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	1
0x92 0a – Charge Pump ON, Fault Mode DISABLE, HS1 – MS1 and HS2 – MS2	9				2				0				a			
	1	0	0	1	0	0	1	0	0	0	0	0	1	0	1	0
0x92 0c – Charge Pump ON, Fault Mode DISABLE, MS1 – LS1 and MS2 – LS2	9				2				0				c			
	1	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0

One Device Control



Write data 0x1203 (SDI) followed by read data to verify latched data 0x1203(SDO)

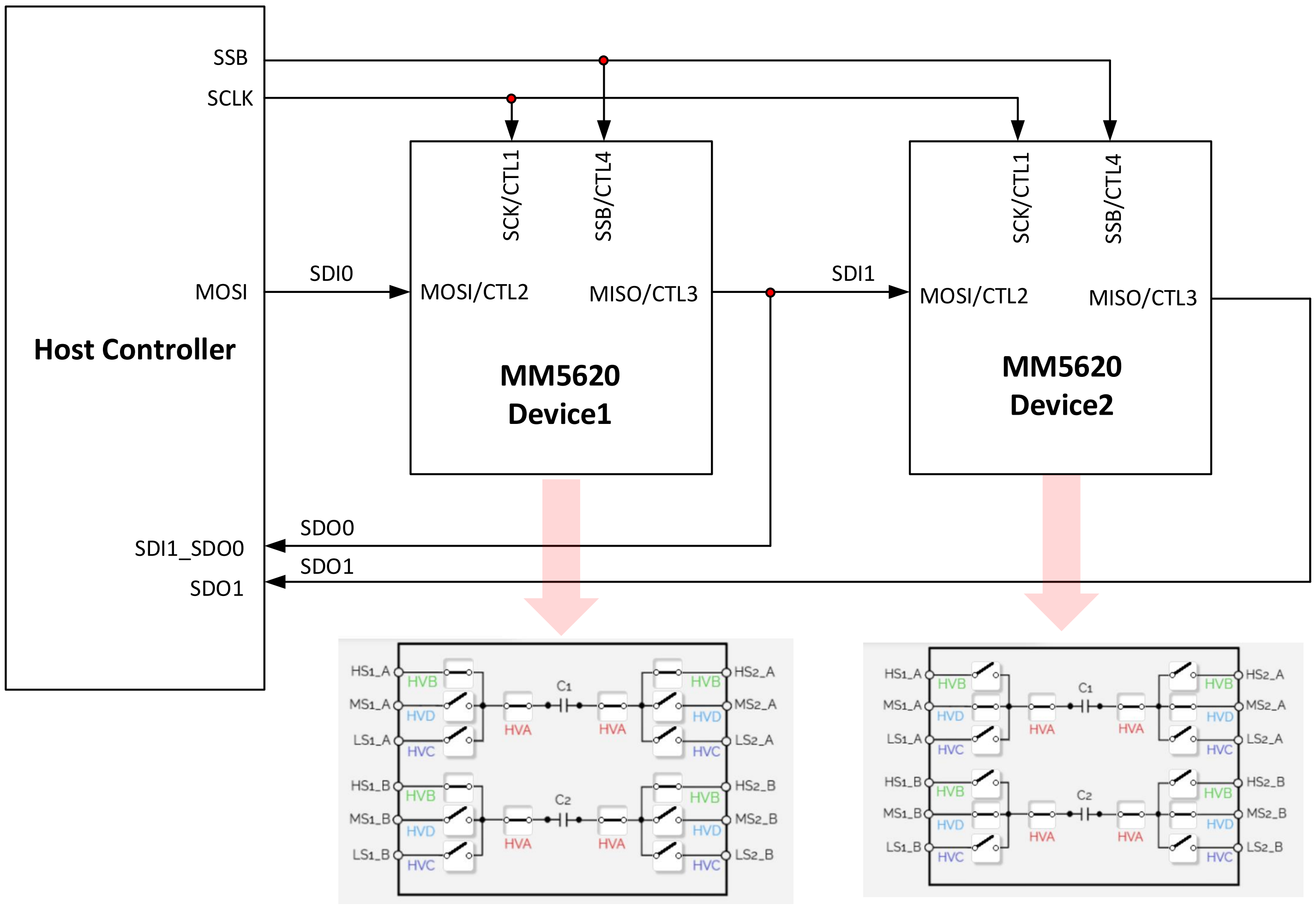
One Device Control Write



MSB is "1"
Write operation

Write 1 word(SDI) and Read it back (SDO)

MM5620/MM5622 Daisy Chain Example: 2 Devices



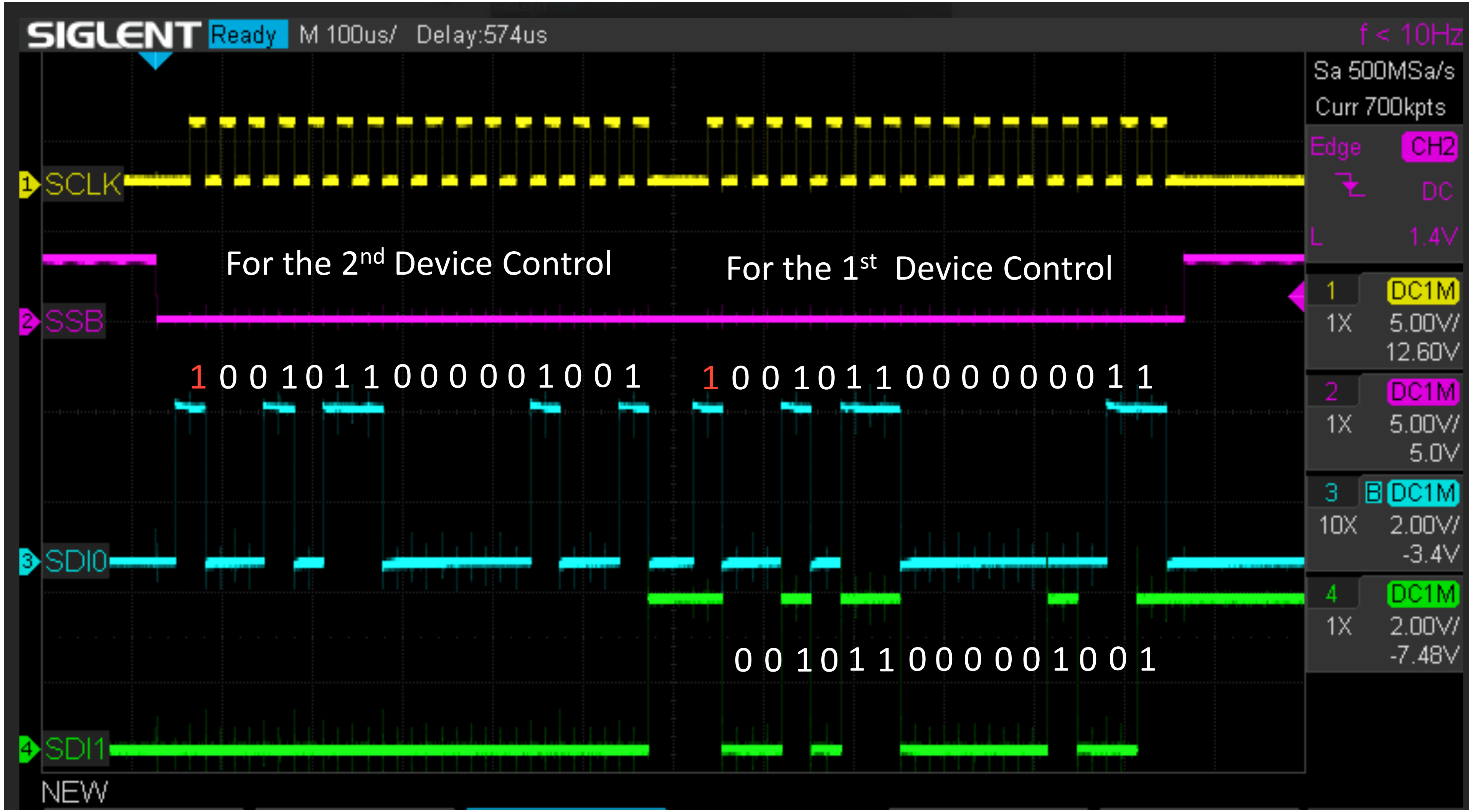
Device 1:
HVA and HVB ON
(HS1 – HS2 ON)

Device 2:
HVA and HVD ON
(MS1 – MS2 ON)

Status Register				Switch State
Bit3	Bit2	Bit1	Bit 0	
HVD	HVC	HVB	HVA	
0	0	0	0	ALL OFF (OPEN)
0	0	1	1	HS1 – HS2
0	1	0	1	LS1 – LS2
0	1	1	0	HS1 – LS1 and HS2 – LS2
1	0	0	1	MS1 – MS2
1	0	1	0	HS1 – MS1 and HS2 – MS2
1	1	0	0	MS1 – LS1 and MS2 – LS2
1	1	1	1	ALL ON (CLOSED)

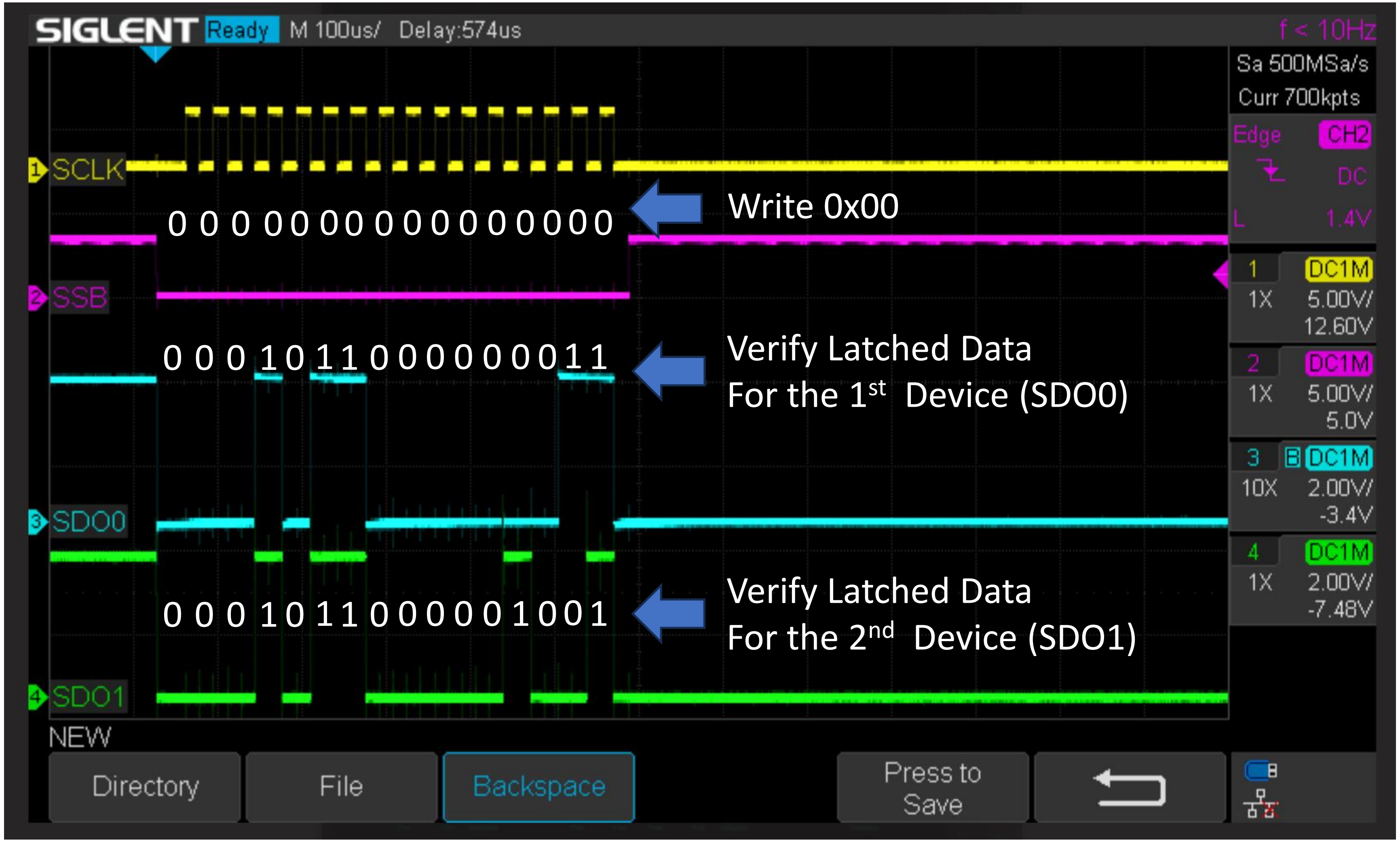
Status Register (Lower 4 bits)

MM5620/MM5622 Daisy Chain Example: 2 Devices



Write 2 words (SDI0) and Monitor SDI1(SDO0)

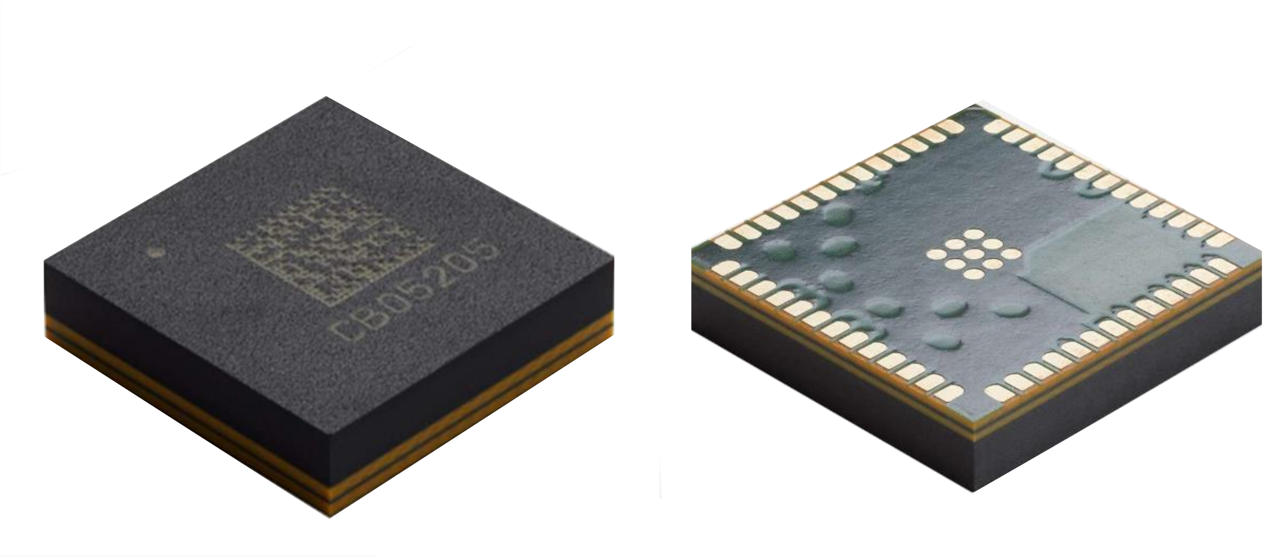
MM5620/MM5622 Daisy Chain Example: 2 Devices (continued)



Write 0x00 to read latched data and Verify SDO0 and SDO1

The Ideal Switch®

MM5600 – 40 Gbps High-Speed Differential Switch



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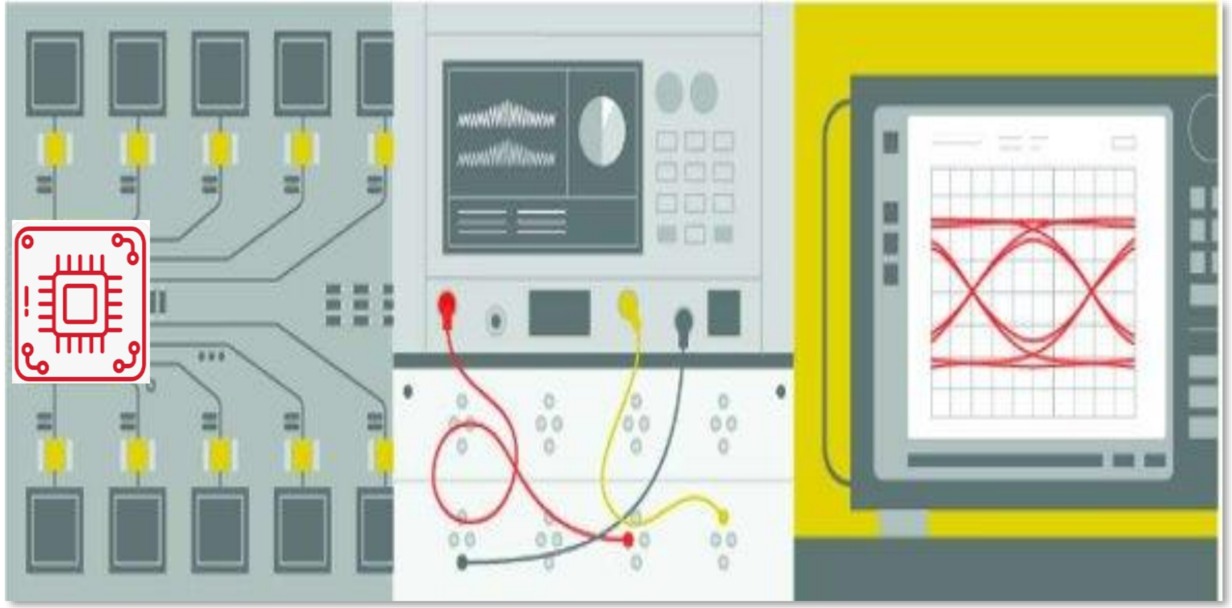
MM5620 – Target Markets & Applications

Target Markets

- Automated Test Equipment
- Measurement Equipment
- Semiconductor Final Package Testing
- Compliance and Loopback Testing
- Aerospace & Defense Equipment



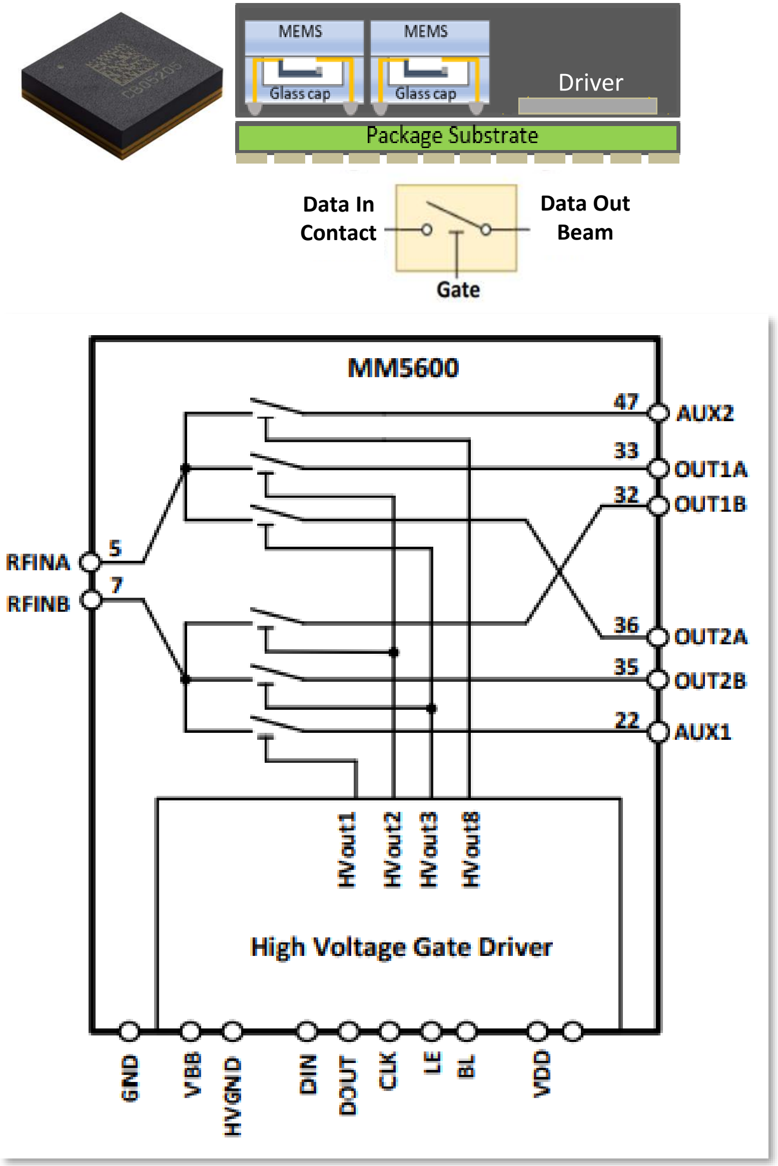
Target Applications

- High-Speed Digital SoC Testing

  PCIe Gen 5, SerDes, USBx.x, InfiniBand, HDMI…
- Optical-Electrical Module Testing
- High Speed Signal Routing
- Differential Switch Matrices

MM5600 – Product Highlights

- DPDT high-speed differential signaling
- DC to 20 GHz range, up to 40 Gbps
- Optimized for PCIe Gen 4 & 5, SerDes
- Auxiliary ports for loopback & signal monitor
- Integrated driver, ESD protection
- Power supply 89 V (bias), 5 V (driver)
- SPI* interface
- High reliability >3B switching cycles
- 8 mm x 8 mm LGA



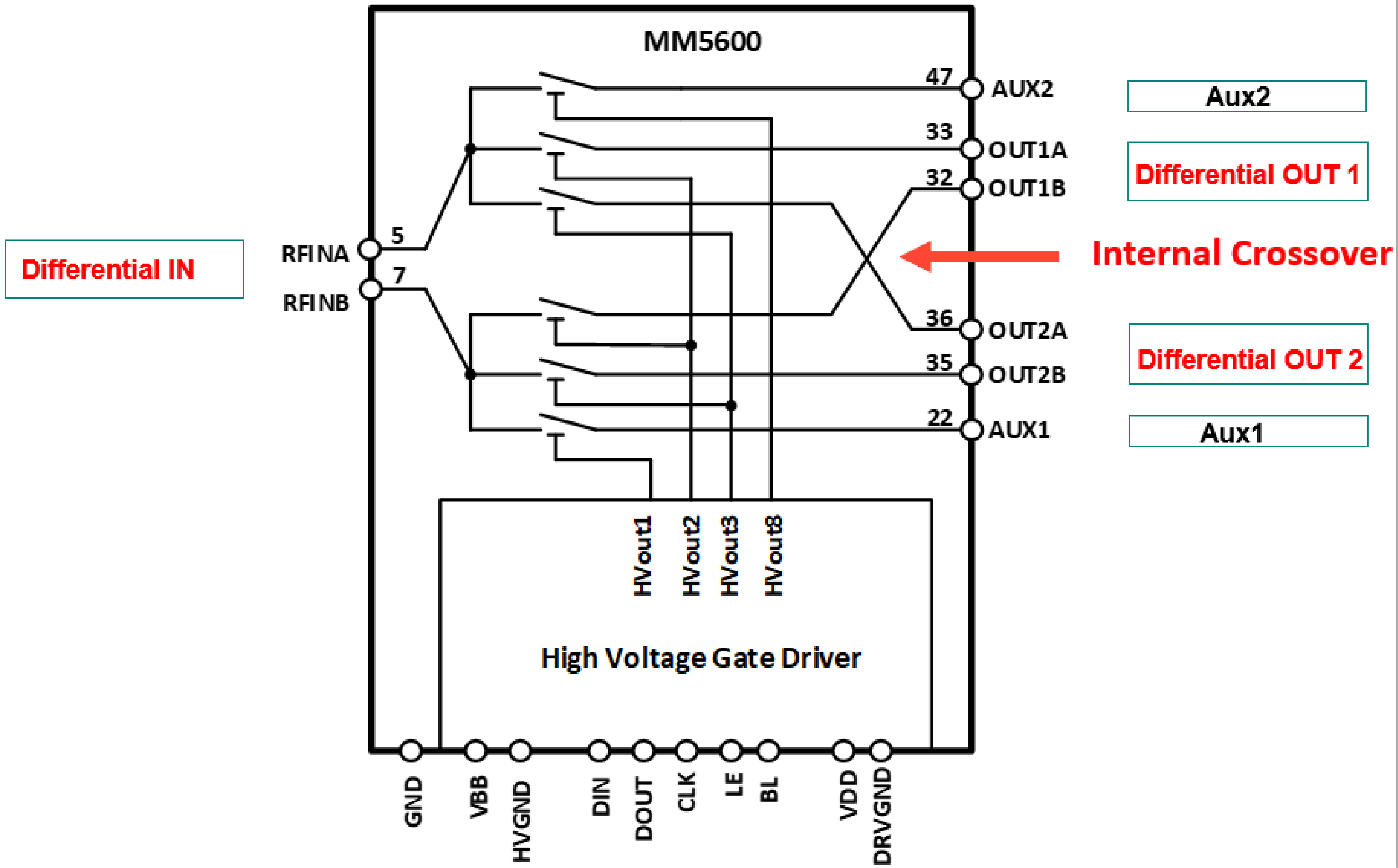
[Menlo MM5600 Datasheet (menlomicro.com)](menlomicro.com)

[MM5600-01NDB_Qual_and_Characterization_Report.pdf (menlomicro.com)](menlomicro.com)

*SPI control signals: Data, Clock, Blank, Latch

MM5600 - DPDT Differential Switch Block Diagram

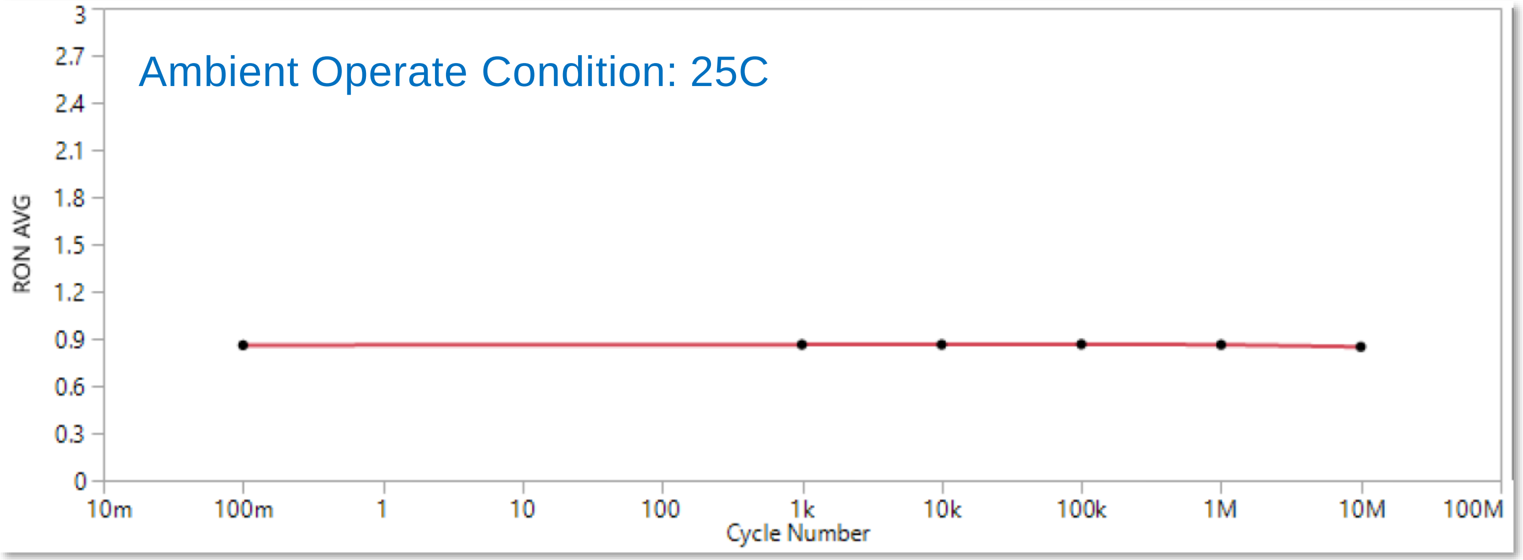
With Integrated Driver and Dual Auxiliary Ports

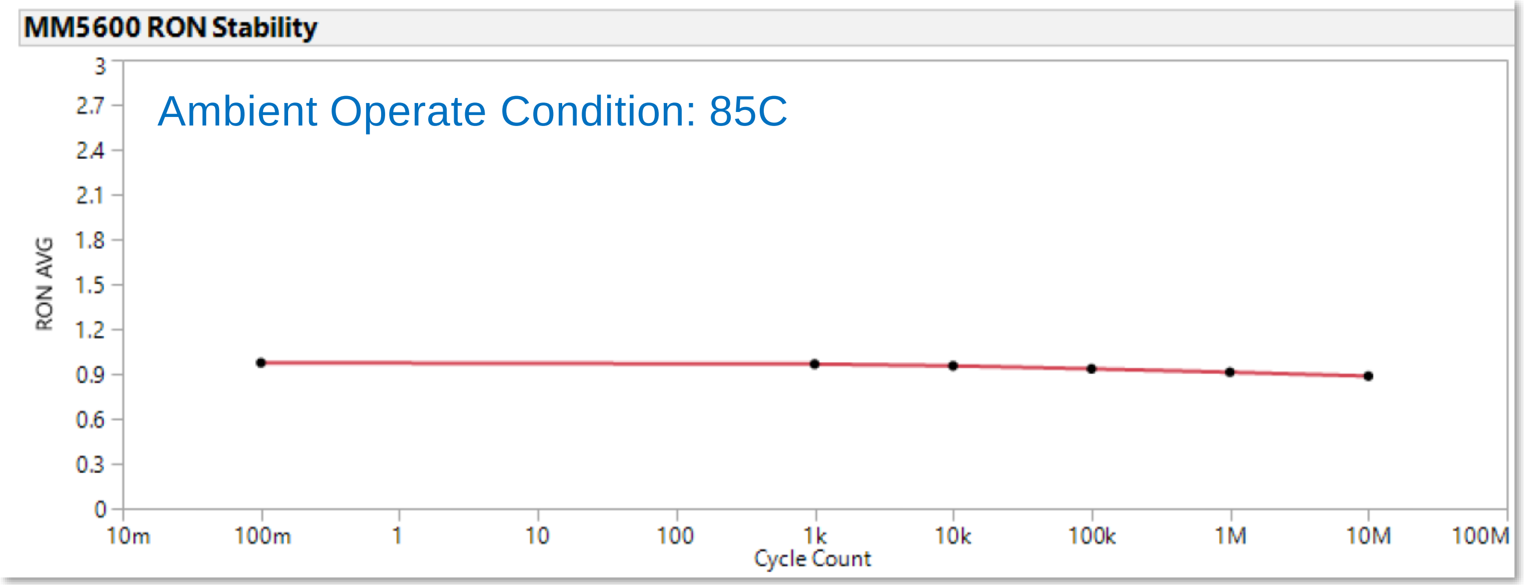


Pin #	Pin Name	Description
1,2,3,4,6,8,9,21,23,24,25,26,27,28,29,30,31,34,37,38,39,40,41,42,43,44,45,46,48,49,50,51,52	GND	RF Ground
53,54,55,56,57,58,59,60,61	EPAD	Tie these pins to GND
15	DRVGND	Driver Ground
16	HVGND	High Voltage Ground
11	CLK	Clock
10	BL	Blank
12	LE	Latch Enable
18,20	NC	No Connect
14	DIN	Data In
17	DOUT	Data Out
19	V_{BB}	High Voltage Supply
13	V_{DD}	Logic Supply Voltage
5	RFINA	Differential Input A
7	RFINB	Differential Input B
33	OUT1A	Differential Output 1A
32	OUT1B	Differential Output 1B
36	OUT2A	Differential Output 2A
35	OUT2B	Differential Output 2B
22	LB1/AUX1	Single-ended Output 1
47	LB2/AUX2	Single-ended Output 2

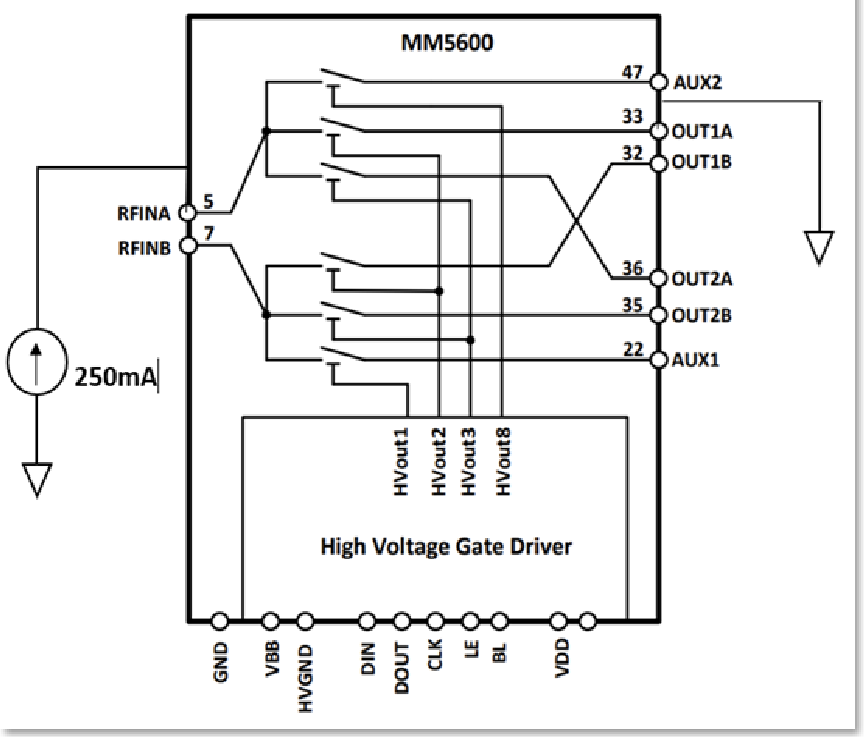
With “cross-over” within the package to provide true differential mux

MM5600 – R_{ON} Reliability & Repeatability Measurements

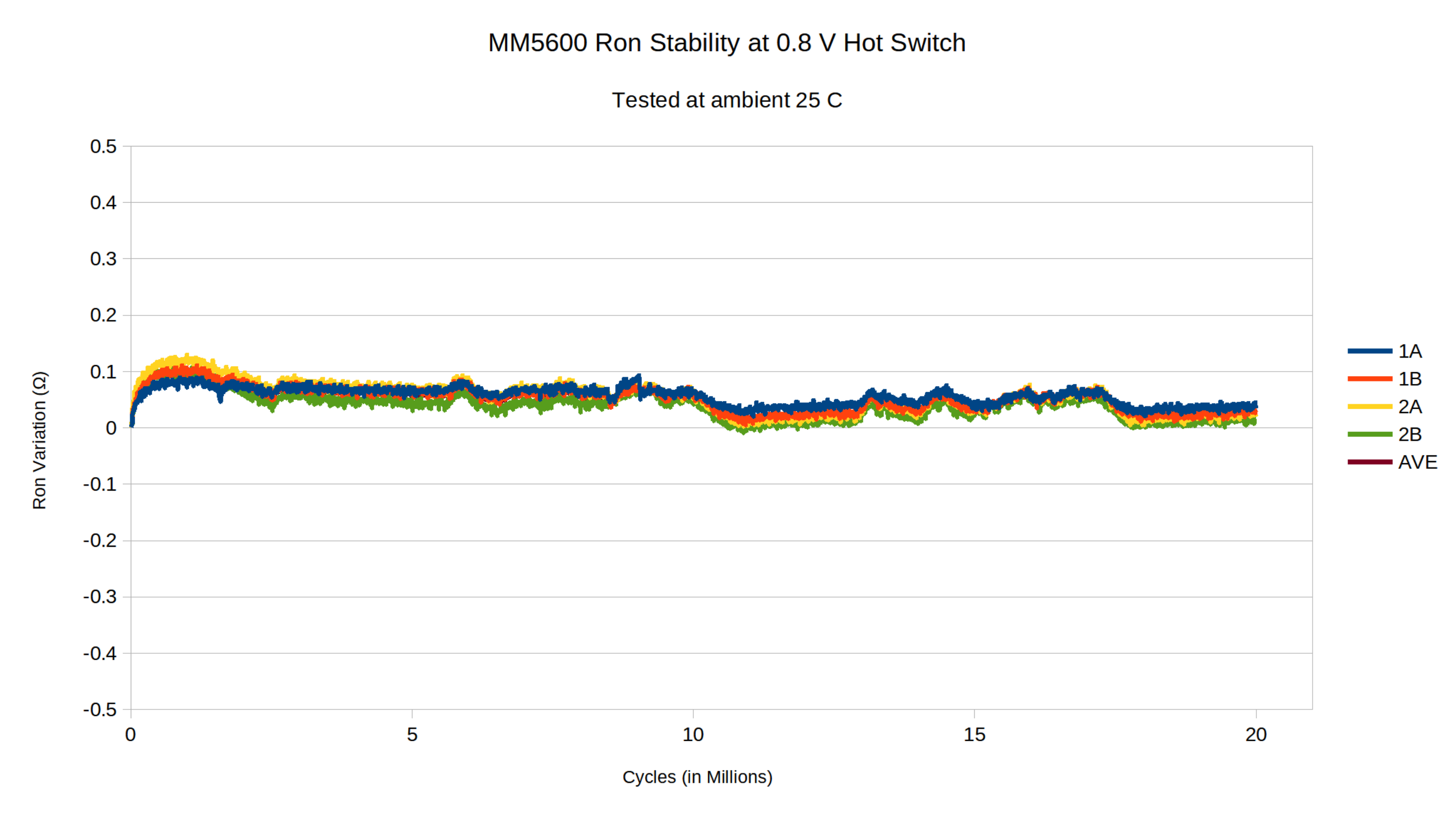




Test Setup

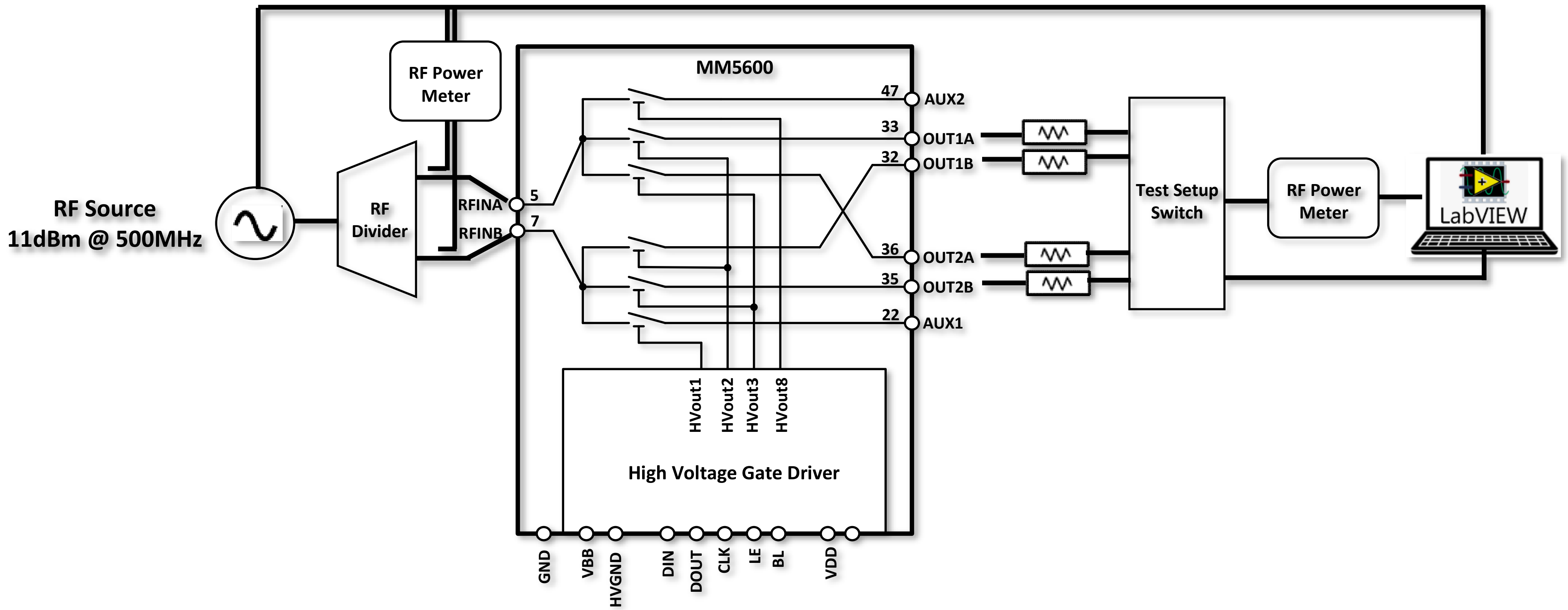


MM5600 – Hot-Switch R_{ON} Measurements



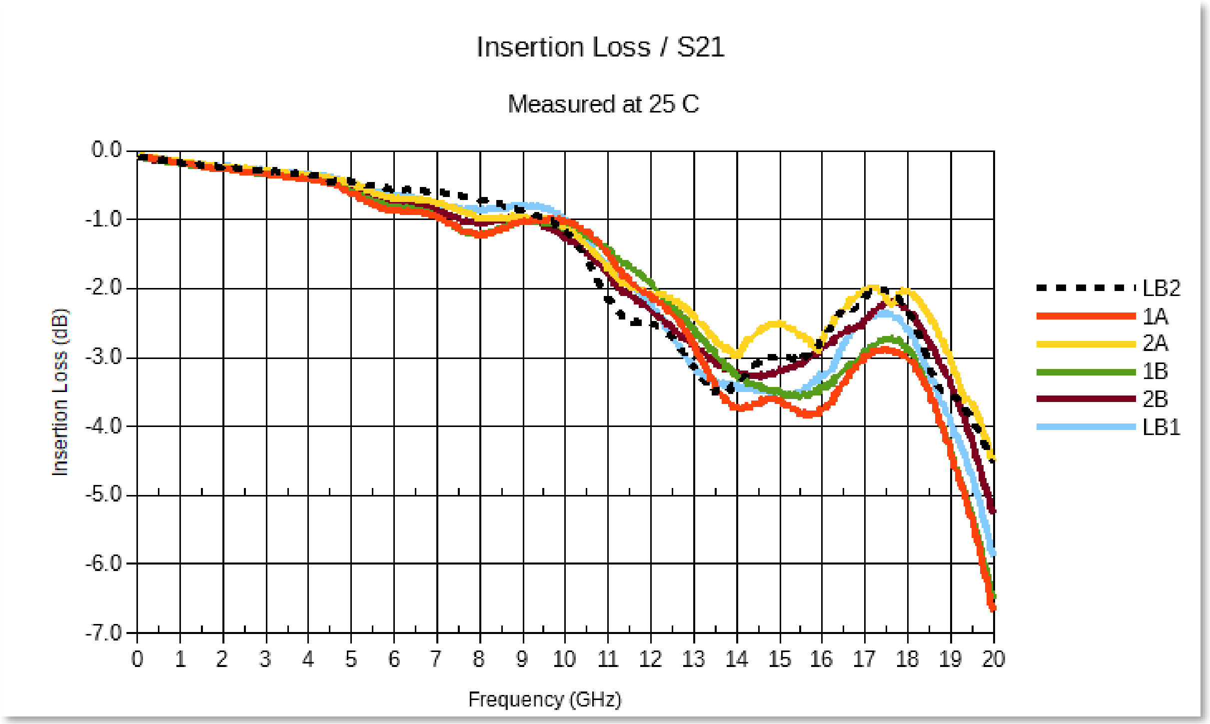
- Measured R_{ON} variation over cycles, with 500 MHz RF signal
- Test data taken from INA to OUT1A, INA to OUT2A, IN2 to OUT2A, IN2 to OUT2B
- R_{ON} Values captured for 20 million cycles at 25°C
- R_{ON} varied by a maximum of ~0.1 Ω over 20 million cycles

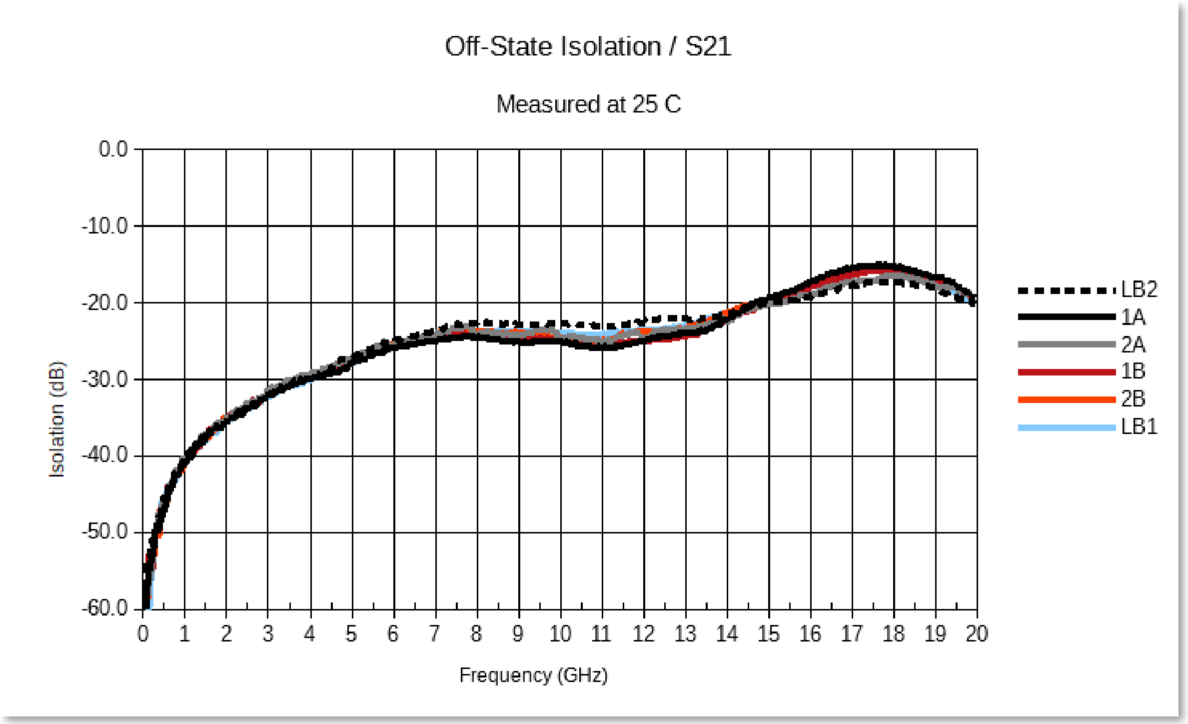
MM5600 – Hot Switch R_{ON} Test Setup



- Hot switched RF signal with 11dBm @ 500 MHz
- RF hot switch test setup with 0.8 V_{RMS} (2.26 V_{P-P}) calculated to approximate a DC signal with 50 Ω load
- R_{ON} values calculated as ΔInsertion $Loss_{50\Omega}$ /I^2_{RMS}
- Measurements were made using SMA cables and RF power meters, recommend using Kelvin clips (4-wires) for accurate DC testing

MM5600 - S-parameter Measurements

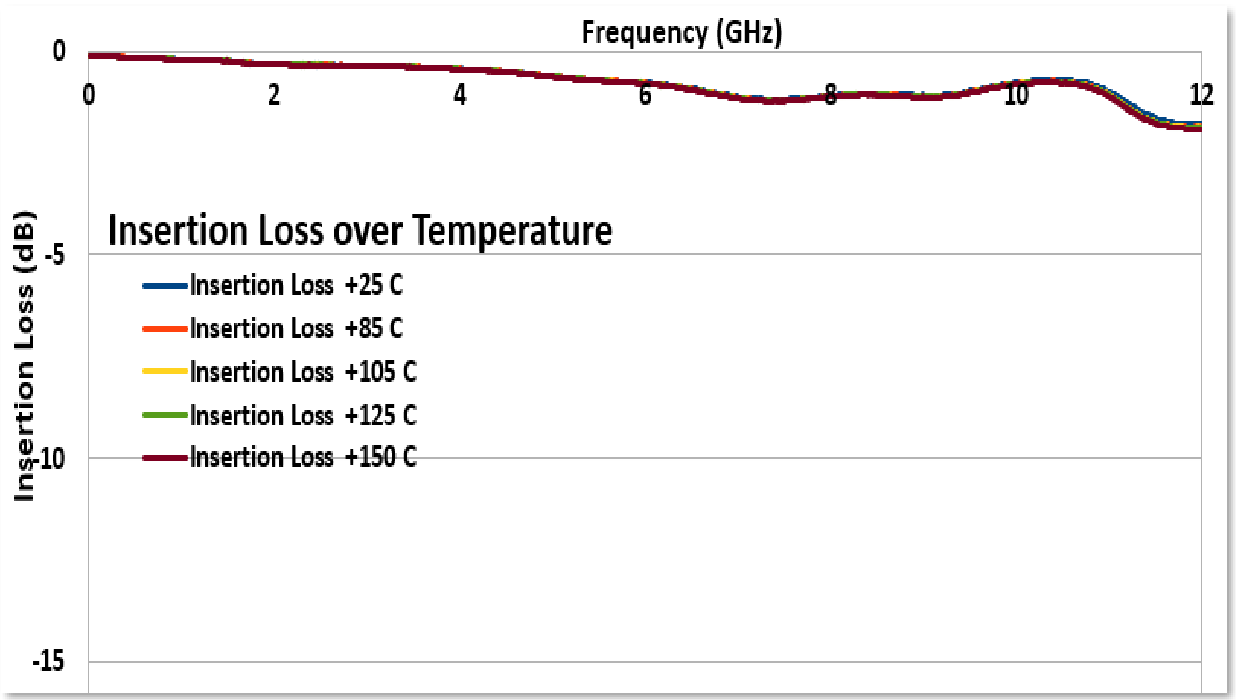


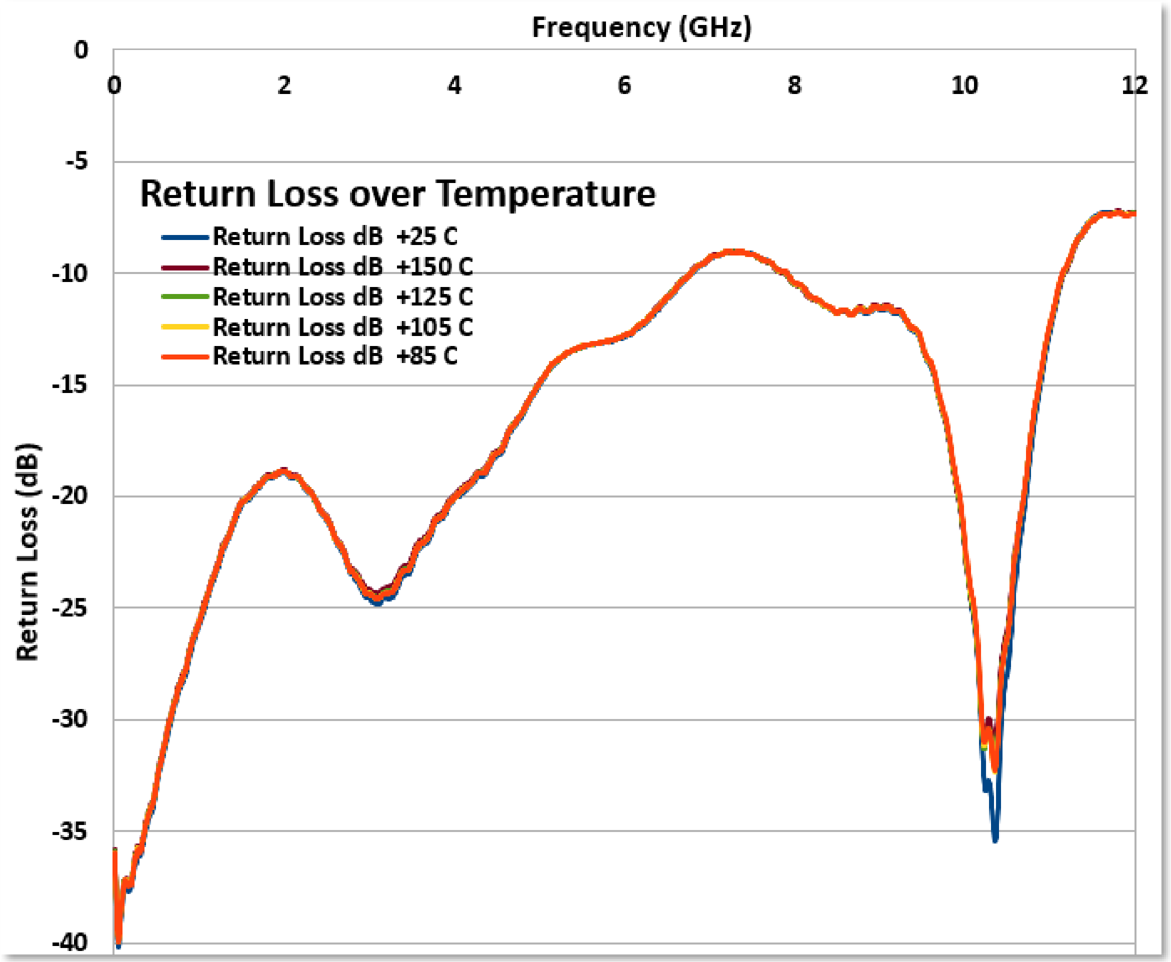


- De-embedded performances on MM5600 Differential EVK
- IL 3.5 dB @ 16 GHz Nyquist BW for 32 Gbps PCIe/ ISO 19 dB @ 16 GHz

MM5600 - S-parameter Measurements Over Temperature

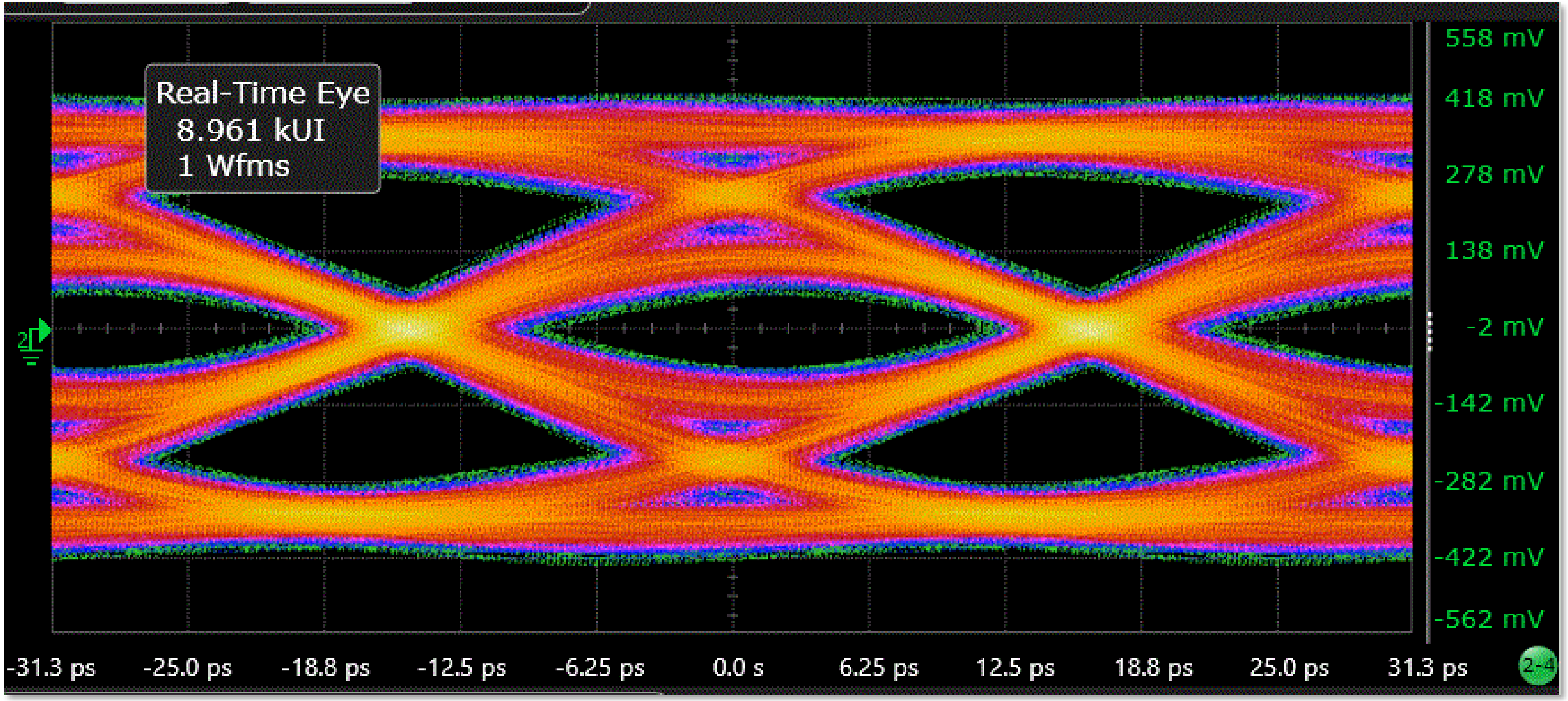
Tight S-Parameter stability channel-to-channel*





*Data is for performance references and DOES NOT imply MM5600 is rated to operate at temperatures above 85C

MM5600 – Loopback Eye-Diagram Performance*

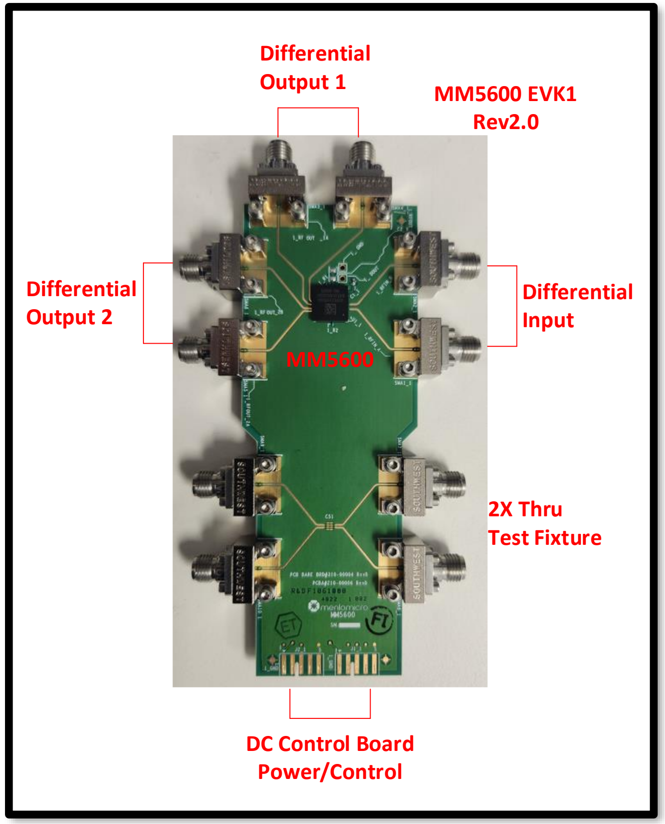


*RF connectors and RF traces are not de-embedded

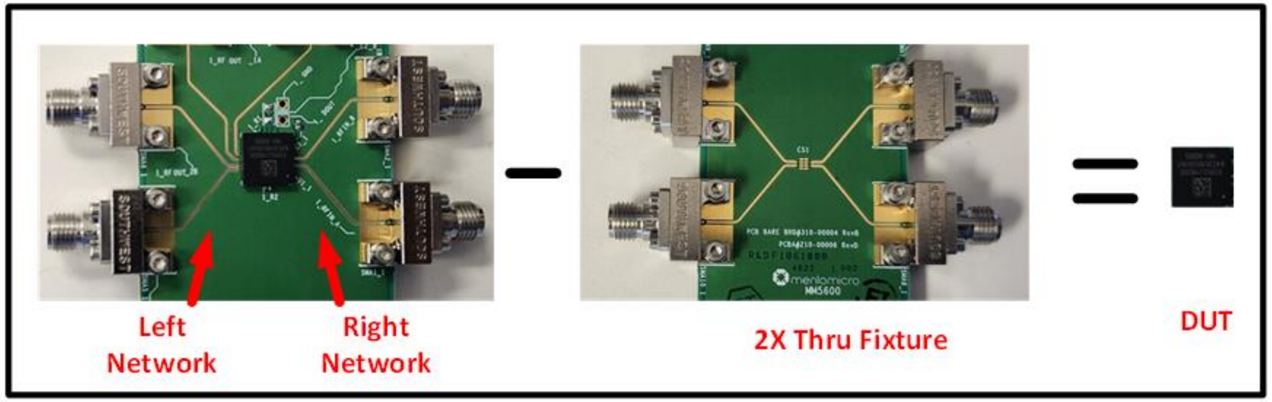
Bit rate (Gbps)	Eye Height (mV)	Eye Width (ps)
32.0	108.0	20.2

MM5600 - De-Embedding Technique with 2x-Thru De-Embedding

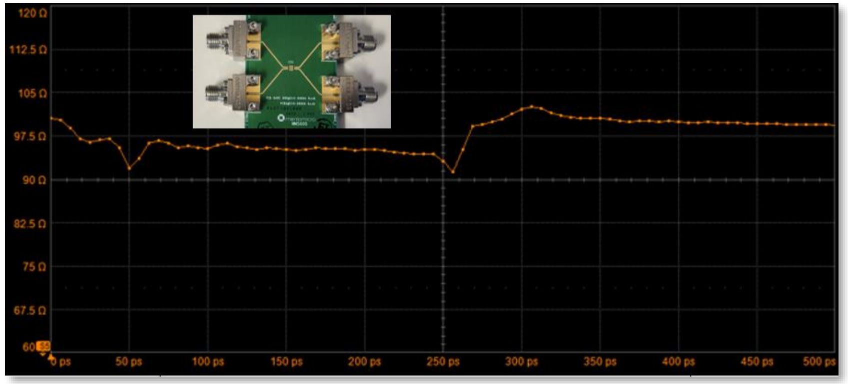
- As the device under test (DUT) is typically mounted on a board with input/output RF traces and connectors we want to de-embed the measured performance to obtain the true device under test performance



MM5600 EVK1 Rev2.0

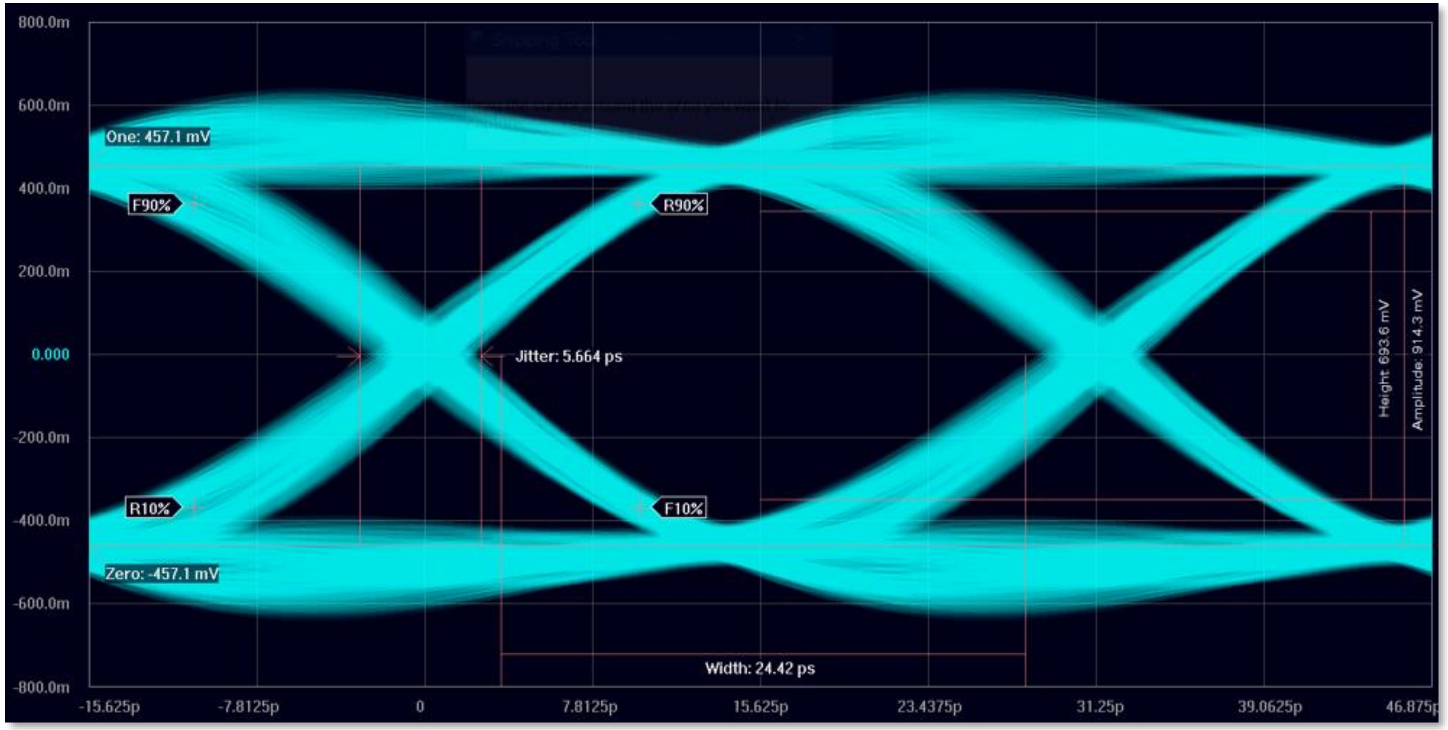


2x-thru de-embedding



TDR measurement

MM5600 - EVK1 Rev2– Signal Integrity Measurement Result

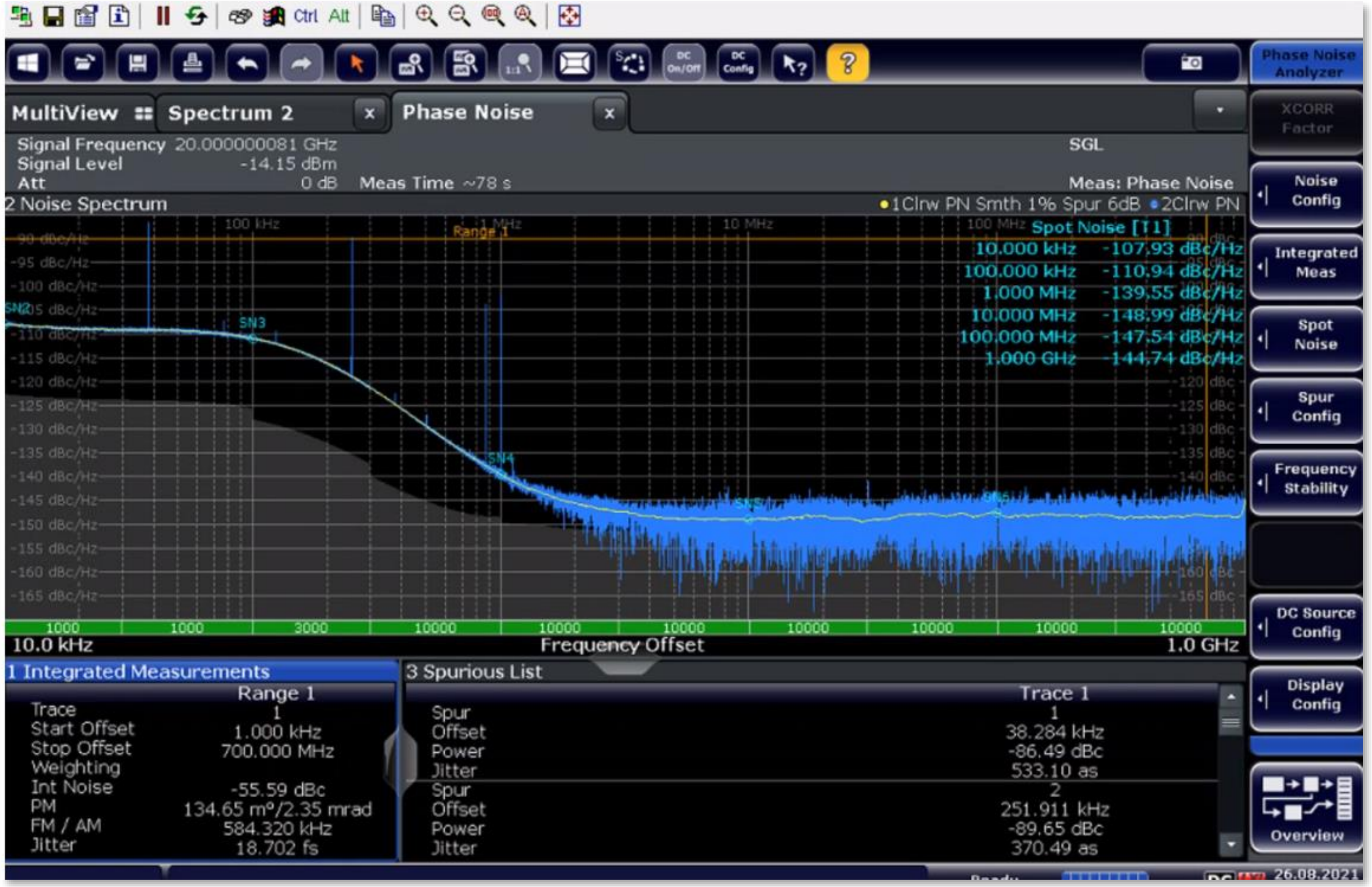


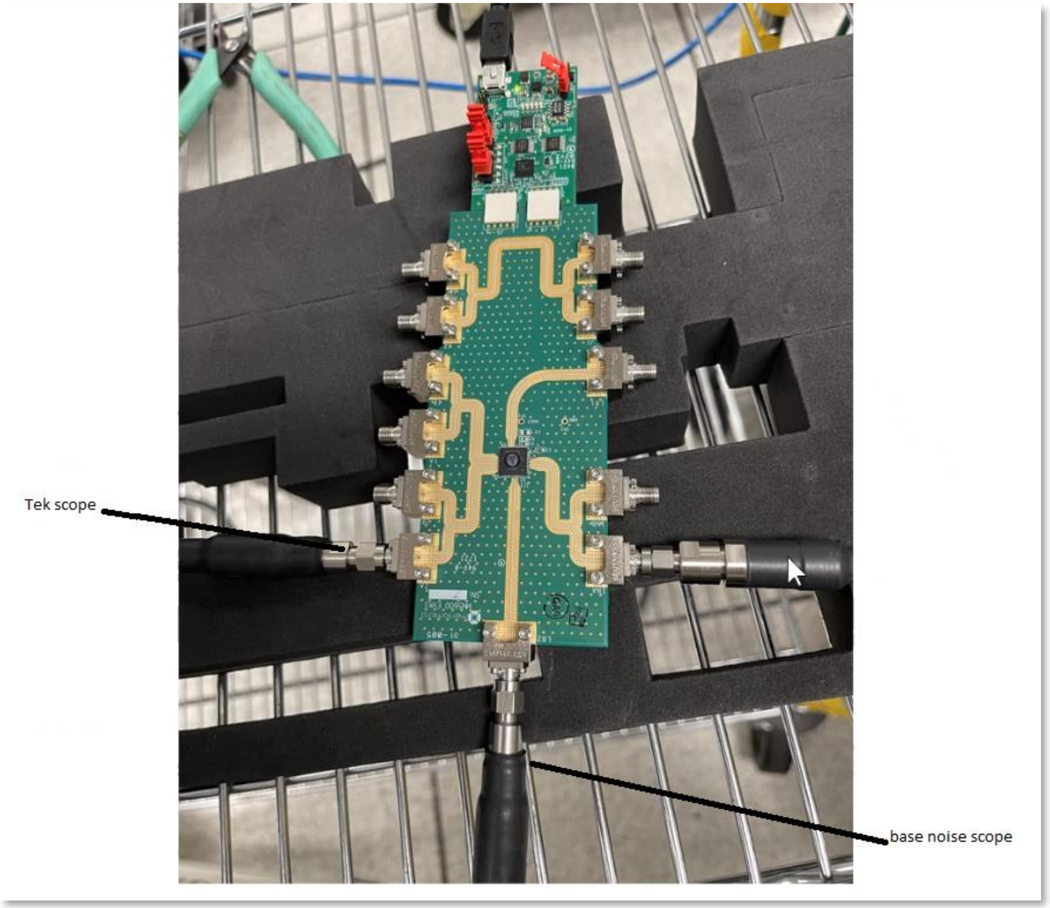
32 Gbps Eye Diagram Performance

Test conditions for measurements above are

- 2^{15}-1 PRBS signal
- NRZ, 32GBps
- PRBS output is 1000mVp-p
- RF connector and RF traces are de-embedded

MM5600 - Phase Noise Measurements*





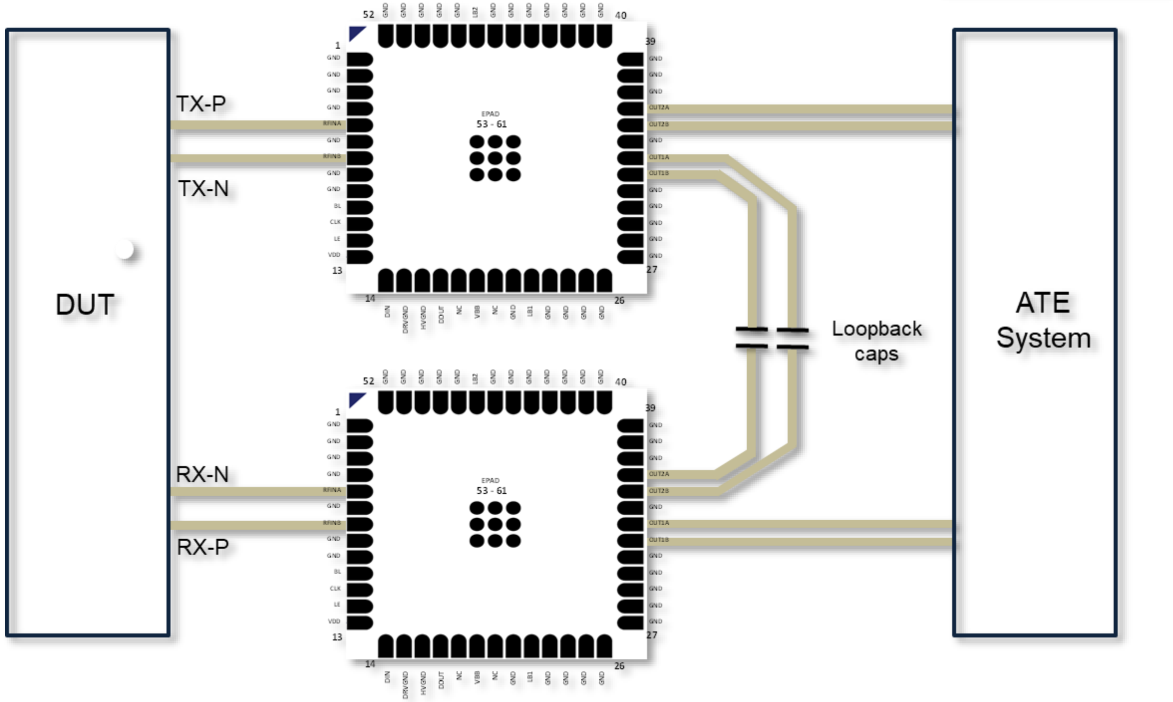
MM5600 EVK Board – Test Setup

- Ultra low phase noise and jitter: -140 dBc @1 MHz offset, <20 fs jitter
- Measured on the R&S FSW Signal Analyzer with Phase Noise Option

*Test results courtesy of NXP

MM5600 - Loopback Test Setup Block Diagram

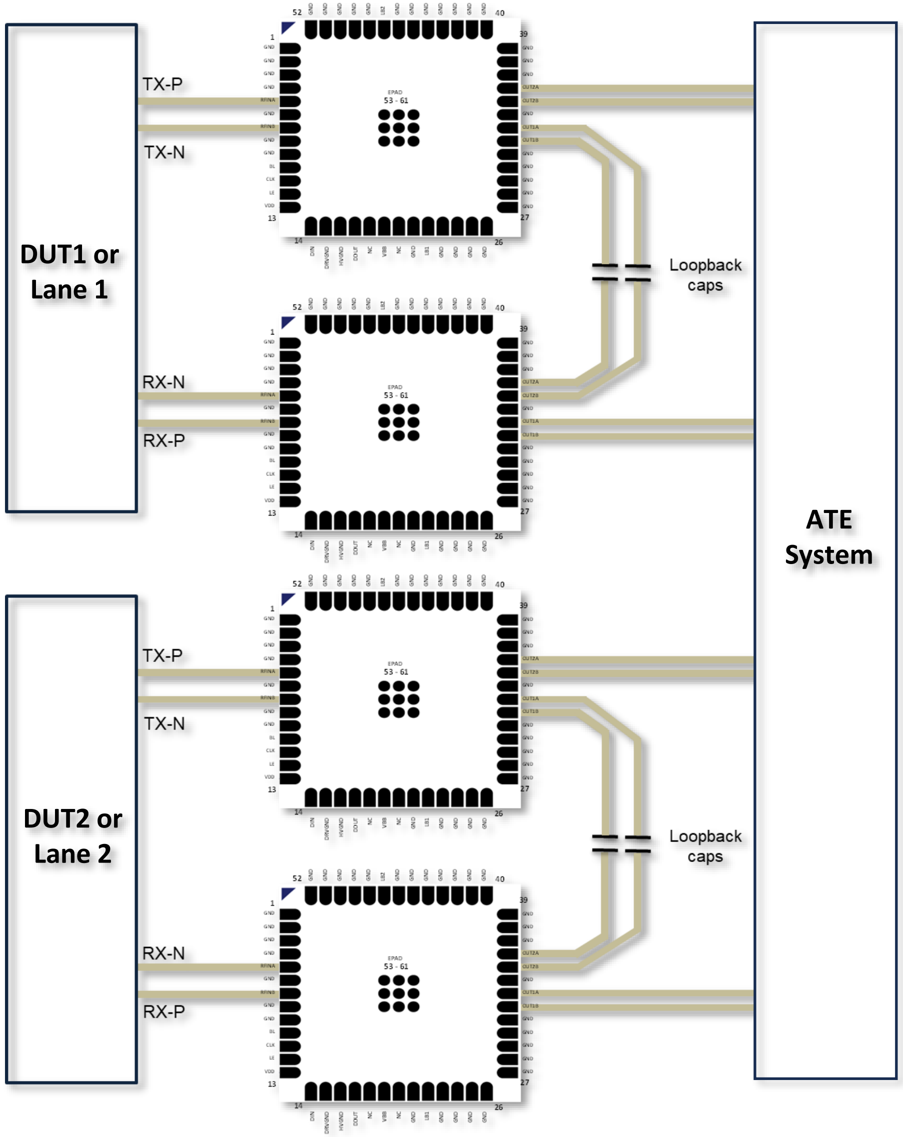
- Utilizing two MM5600 Differential switches configured in a dual DPDT configuration with loopback
- Supports up to 40 Gbps data rates to meet the latest PCIe Gen 5 requirements
- Board design optimized for low-loss RF performance



2 x MM5600 (8mm x 8mm LGA 0.5mm pitch) Top-Down View

MM5600 – Double Density Parallel Loopback Test

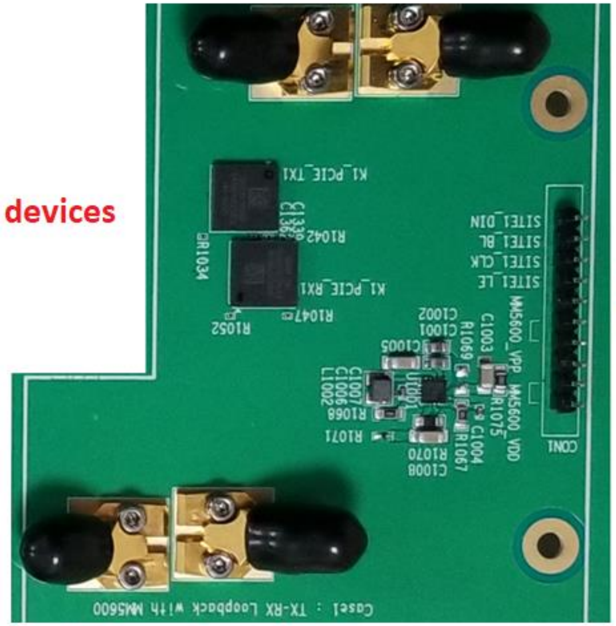
- Utilizing four MM5600 Differential switches configured in a dual DPDT configuration with parallel loopback and ATE tests
- Supports up to 40 Gbps data rates to meet the latest PCIe Gen 5 requirements
- Real time double density parallel tests to reduce testing cost



MM5600 - Loopback Test Board

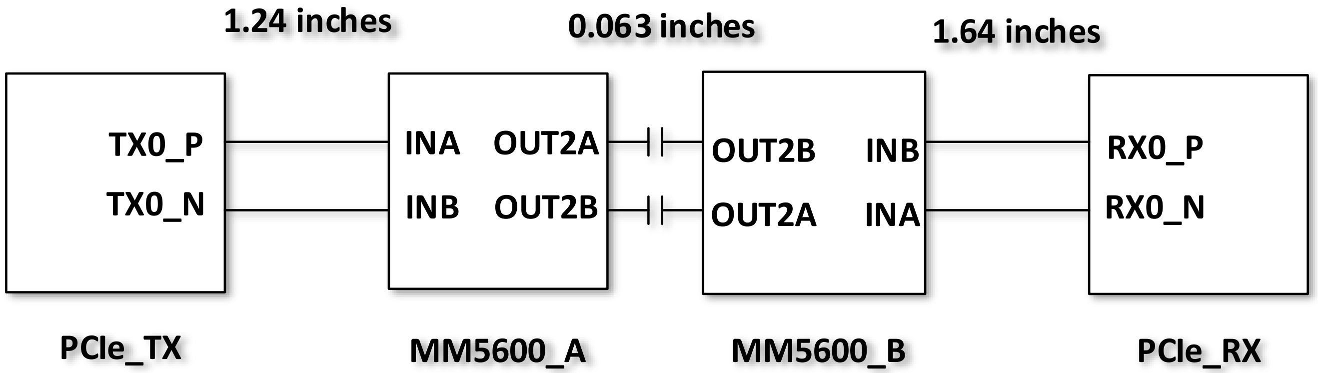
1.85mm female RF connectors

Two MM5600 devices



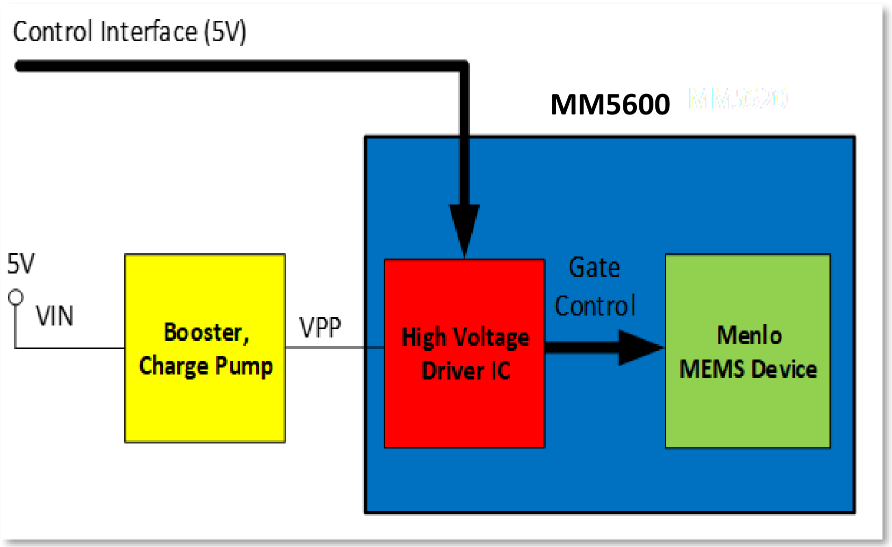
On-board charge pump ckt and control interafce

1.85mm female RF connectors

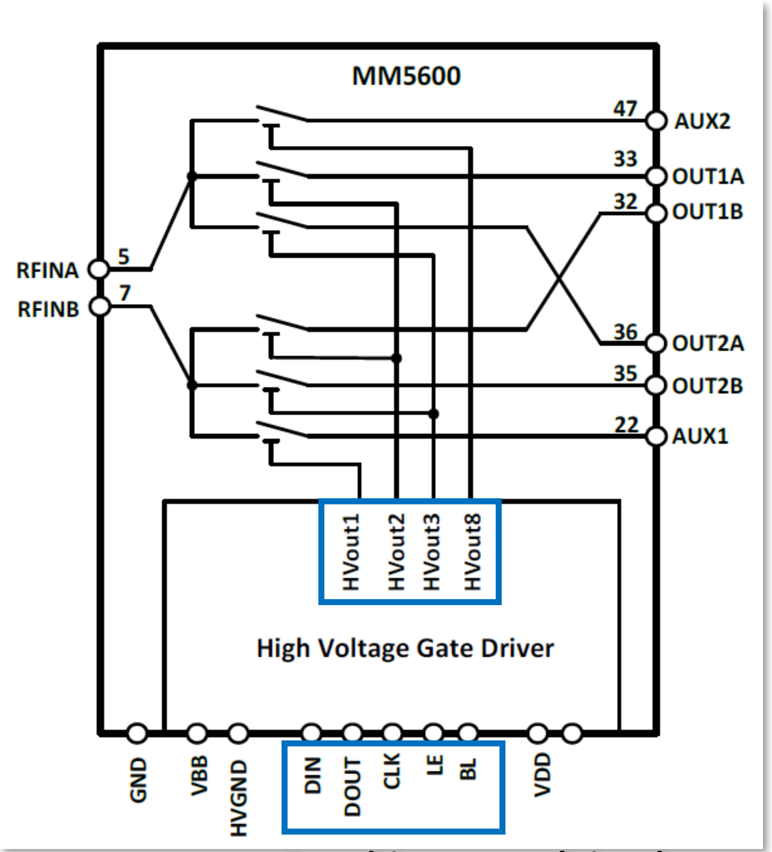


MM5600 - MEMS Switch Control Block Diagram

High voltage gate driver is controlled via serial-to-parallel interface driving high voltage gate lines of the switches



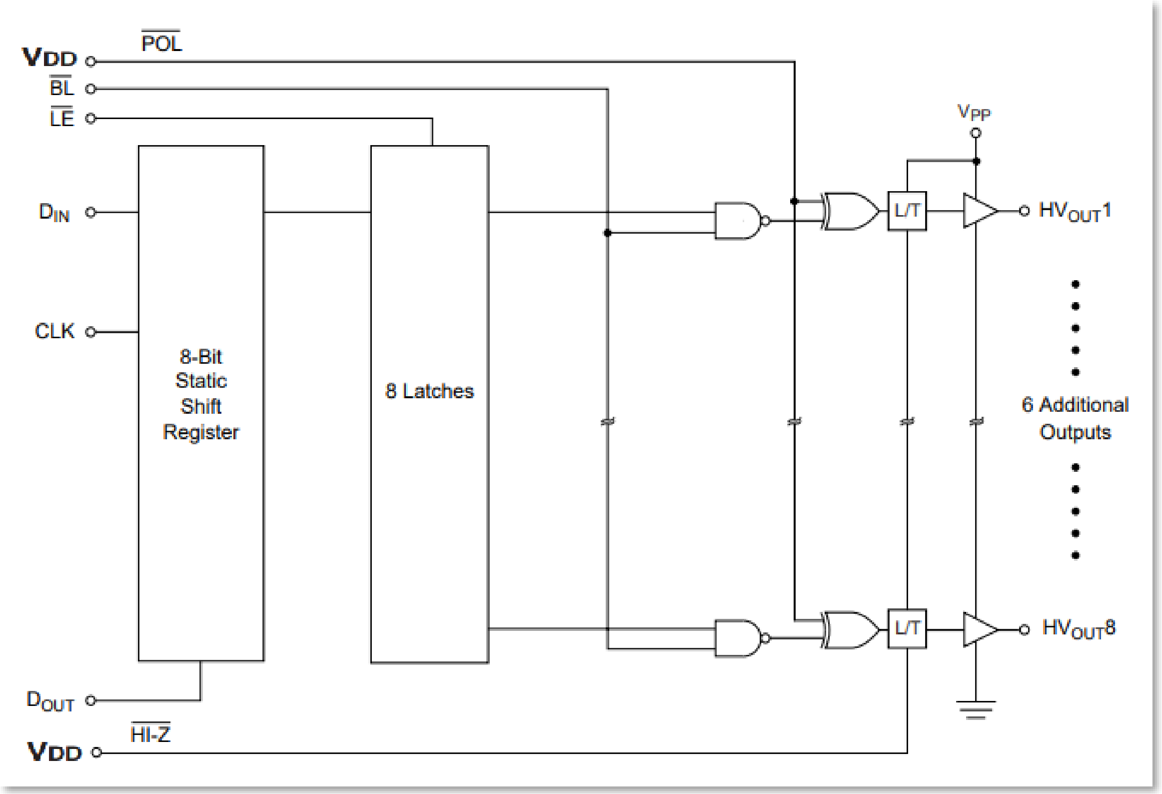
Switch Control Block Diagram



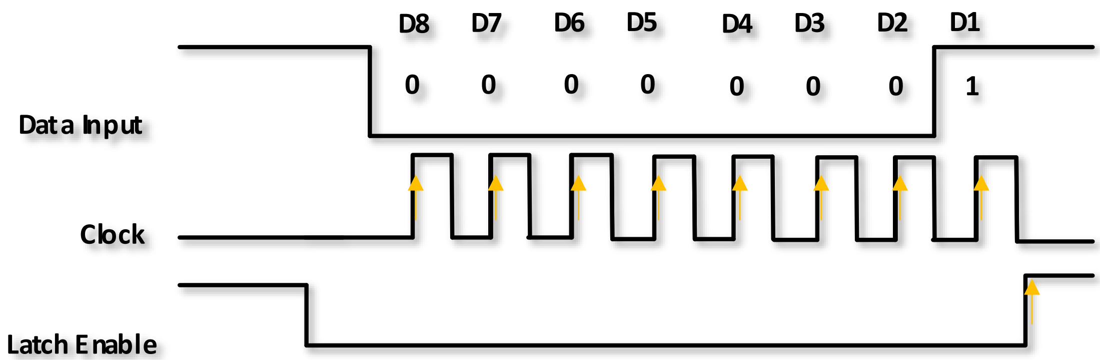
Gate driver control signals
DIN, DOUT, CLK, LE, BL
(MOSI, MISO, Chip Select not required)

Gate Driver Digital Section of the Block Diagram

The built-in driver has an 8-bit shift register and latch. The bits are shifted from top to bottom at every clock edge. And the outputs are latched at when the LE signal is applied

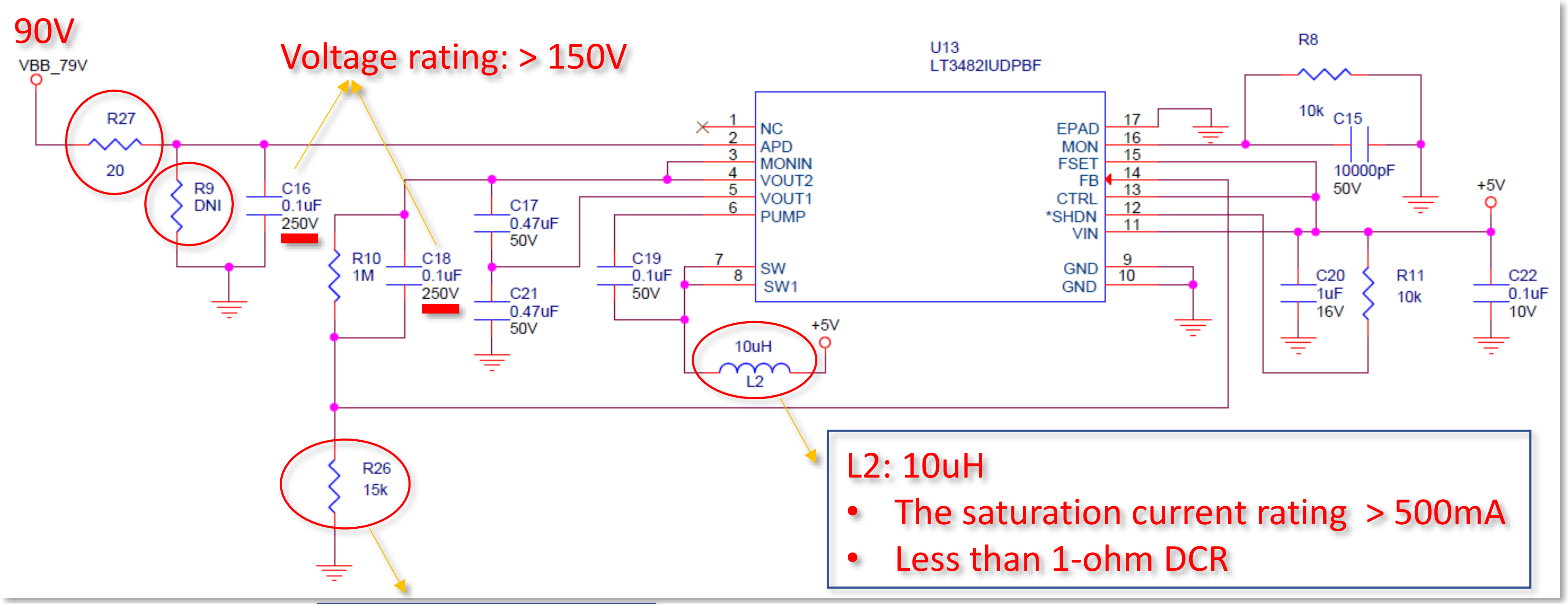


HV[8,3,2,1] used



Gate control (AUX1 ON)

MM5600 – Charge Pump Circuit Schematics



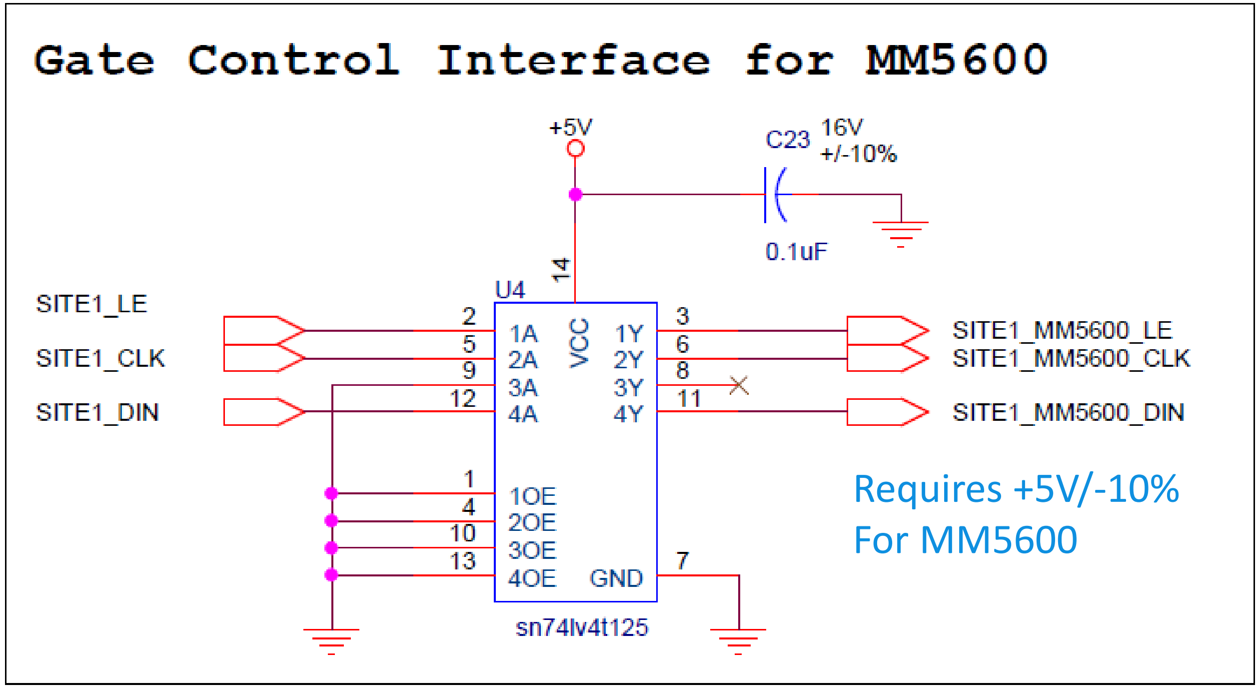
Feedback Resistor
- 13.7K: 90V

[LT3482 Datasheet and Product Info | Analog Devices]

MM5600 - Logic Supply Voltage Schematics

- Driver Voltage Supply VDD: 5V+/-10%
- May require voltage translator (from < +4.5V to +5V)

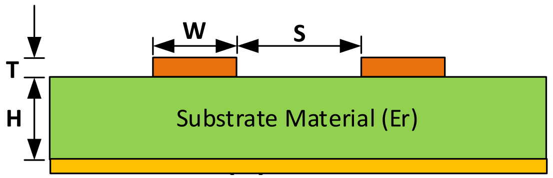
When < +4.5V
Voltage translator is required
(ie: SN74LV4T125)



Requires +5V/-10%
For MM5600

High-Speed Digital PCB Design

- To achieve a good high-speed PCB design to meet the specific design target, it is very important to get deep understanding of your fabrication houses' capability and details of their design rules in advance, then work very closely together with them.
- Most high-speed differential lines use either an edge-coupled microstrip or an edge-coupled stripline.



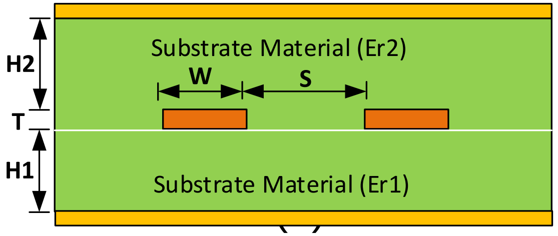


Figure: T(Copper Thickness), W(Trace Width), S (Spacing), H (Substrate Height), and B (Substrate height) (a) edge-coupled microstrip (b) edge-coupled stripline

- It is important to choose better dielectric material with low dielectric constant, low-loss tangent, better surface roughness, Reverse Treated Copper Foil, and better PCB finish (plating method) such as EPIG, ISIG, EPAG, etc. if the design has high-speed routing on top/bottom layer.

High-Speed Digital PCB Design

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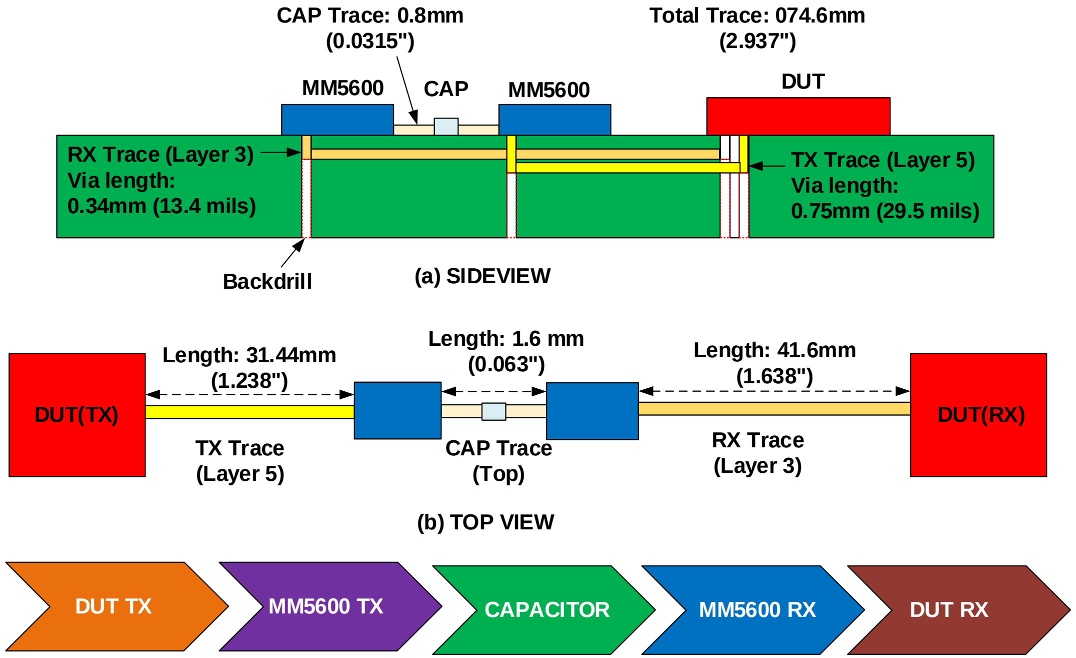
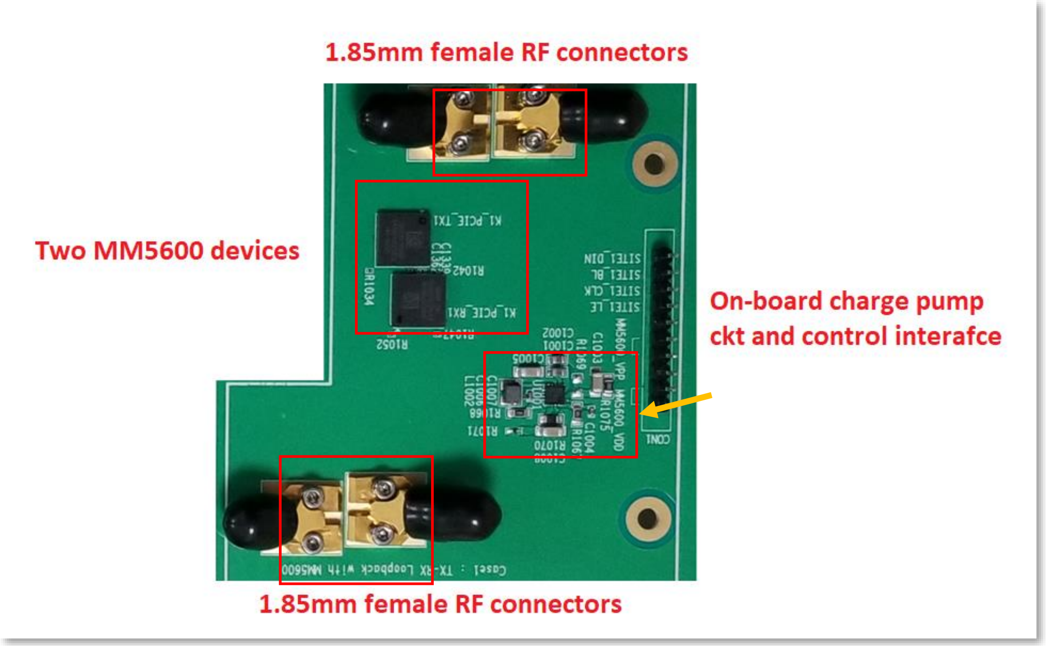
- There are two MM5600 devices used for the loopback functionality. These need to be placed as close as possible to each other. To optimize transmission line design, wider and shorter traces are better to minimize the insertion loss.
- For the differential signals, routing should be smooth with minimum bends and tight length matching is required.
- To provide a proper de-embedding, the 2x-through needs to be implemented with symmetrical routing and placement.
- Stitching vias are required to be placed along all the high-speed routing from DUT to Connectors. If space allows, it is ideal to implement two rows of stitching vias along the RF signals routing.
- Optimizing via transitions is necessary to minimize the impedance mismatch. A TDR simulation using 3D EM tools is a good method to check the impedance of vias and optimize it.
- Soldermask needs to be removed on high-speed traces.
- Although it takes additional time, confirmation by running post-layout full 3D EM simulation, to obtain s-parameter, TDR, and eye diagram results, is a must to ensure that the board layout can meet the requirements.

MM5600 Loopback Circuit with Evaluation Board

- A test coupon board to evaluate the high-speed loopback circuit to make sure the load board design can meet the PCIe Gen5.0 requirements.
- Figure (a) shows the sideview of the load board structure and (b) for its topview. This is the first topology, which is the full path case including a charge pump circuit, control interface, and two MM5600 devices, AC coupling caps and four 1.85mm RF connectors.



(a) Load Board Structure (Sideview)
(b) Load Board Structure (Topview)



(b) Load Board Structure (Topview)
MM5600 Loopback test board

MM5600 Evaluation Board Design with Two Topologies

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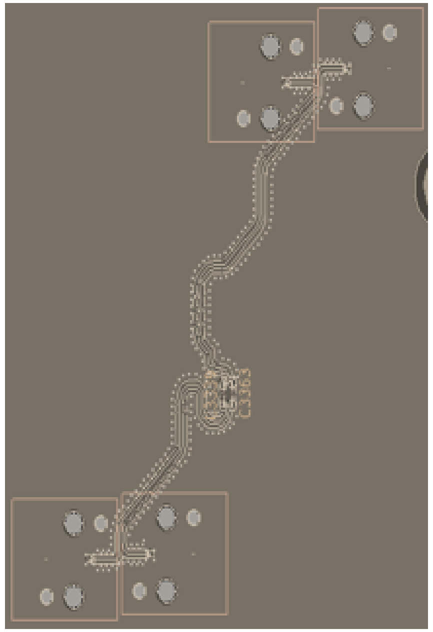
CASE1

CASE2

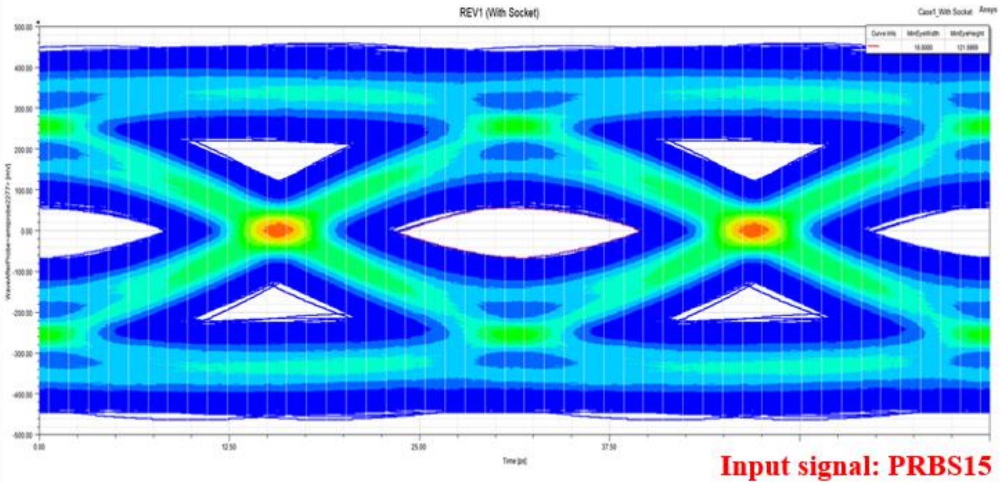


CASE	TOPOLOGY	DETAIL
1	TX-RX Loopback with MM5600	MM5600 mounted and full path case.
2	TX-RX Loopback without MM5600 (Connected to Trace)	MM5600 is not mounted, and the internal circuit of MM5600 is mounted as a trace

Eye-Diagram Performance of the Evaluation Board: Case 1

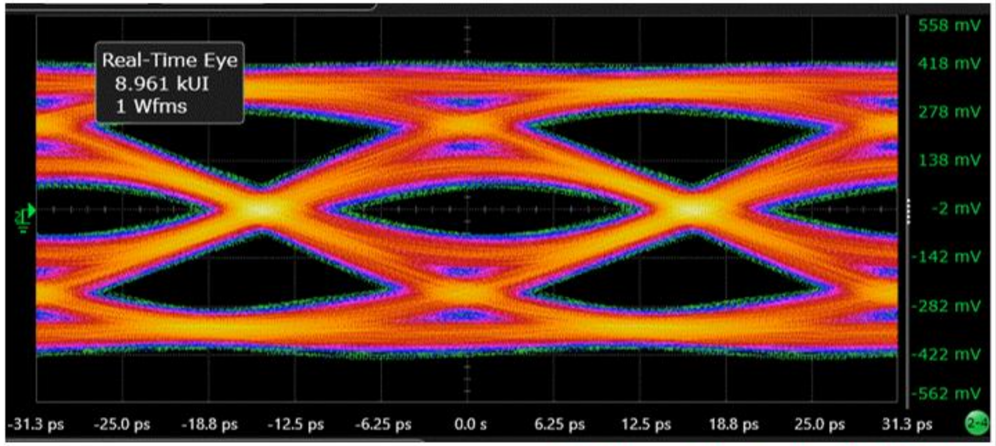
The eye-diagram performance of the evaluation board has been measured and compared with the simulation result for the case 1

Simulation Result
(Included Socket Touchstone File)



Input signal: PRBS15

Measurement Result
(De-embedded 50cm Cable of OSC Side)



All Case of Input signal: PRBS23

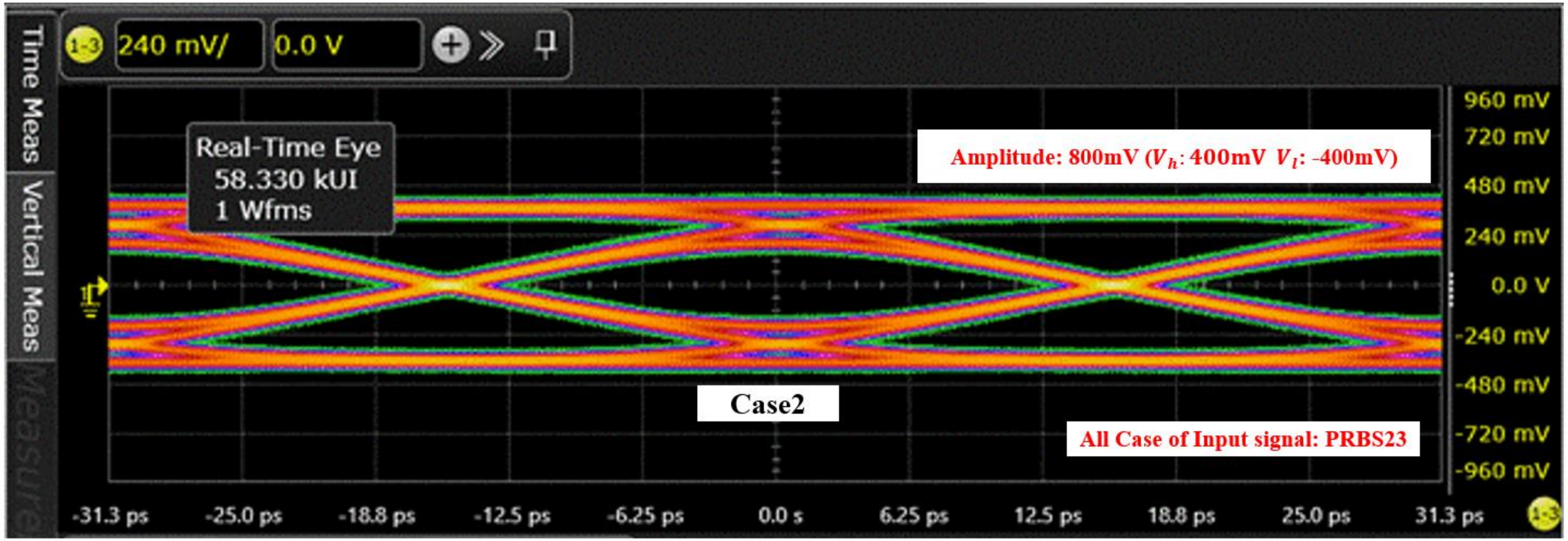
Amplitude: 800mV (V_h: 400mV V_l: -400mV)

Reference Result (Measurement)		Simulation Result		Measurement Result	
Min. Eye Width	Min. Eye Height	Min. Eye Width	Min. Eye Height	Min. Eye Width (% VS Ref.)	Min. Eye Height (% VS Ref.)
26.46ps	510.0mV	15.5ps	121.0mV	20.21ps (76%)	108.0mV (22%)

Figure - Case 1, PCIe Gen5 - 32Gbps Evaluation Result. NRZ, 800mVpp
(a) Simulation Result, PRBS 2^{15}-1, (b) Measured result, PRBS 2^{23}-1

Eye-Diagram Performance of the Evaluation Board: Case 2

The eye-diagram performance of the evaluation board has been measured for the case 2



Reference Result		Measurement Result	
Min. Eye Width	Min. Eye Height	Min. Eye Width (% VS Ref.)	Min. Eye Height (% VS Ref.)
26.46ps	510.0mV	25.00ps (95%)	270.0mV (53%)

Figure - Case 2, 32Gbps Loopback without MM5600 (Connected to Trace), Measured result, NRZ, 800mVpp, PRBS 2^{23}-1

Thank you

Menlo Microsystems, Inc
49 Discovery, Suite 150
Irvine, CA 92618
Menlomicro.com